

5/10-Gb/s Burst-Mode Clock and Data Recovery Based on Semiblind Oversampling for PONs: Theoretical and Experimental

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Abstract—In this paper, we demonstrate a 5/10-Gb/s burst-mode clock and data recovery circuit (BM-CDR) for passive optical network (PON) applications. The BM-CDR is based on a phase-tracking oversampling (semiblind) CDR circuit operated at twice the bit rate and a clock phase aligner that makes use of a simple phase-picking algorithm for automatic clock phase acquisition. The design provides low latency and fast response without requiring a reset signal from the network layer. We experimentally test the proposed BM-CDR in a 20-km PON uplink. The BM-CDR achieves a bit error rate (BER) $< 10^{-10}$ and packet loss ratio (PLR) $< 10^{-6}$ while featuring: 1) instantaneous (0 preamble bit) phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts; 2) BER and PLR sensitivities of -24.2 and -25.4 dBm, respectively; 3) negligible burst-mode sensitivity penalty of 0.8 dB; 4) frequency acquisition range of 242 MHz; 5) consecutive identical digit (CID) immunity of 3100 bits; and 6) dynamic range of 3 dB. With the instantaneous phase acquisition, we predict the physical efficiency of the upstream PON traffic to be 99%. We also present a unified probabilistic theory for conventional CDRs, N times oversampling CDRs in either time or space, and BM-CDRs built from oversampling CDRs. This theory can quantitatively explain the performance of these circuits in terms of the BER and PLR. The theoretical model accounts for the following parameters: 1) silence period, including phase step and CIDs, between consecutive packets; 2) finite frequency offset between the sampling clock and data rate; 3) preamble length; 4) jitter on the sampling clock; and 5) pattern correlator error resistance. On the basis of this theory, we perform a comprehensive theoretical analysis to assess the tradeoffs between these parameters, and compare the results experimentally to validate the theoretical model.

Index Terms—Burst-mode (BM) receiver, clock and data recovery (CDR), clock phase aligner (CPA), passive optical network (PON), probabilistic theory, semiblind oversampling.

Manuscript received September 8, 2009; revised December 2, 2009; accepted January 6, 2010. Date of publication May 10, 2010; date of current version October 6, 2010. This work was supported by Bell Canada and the Natural Sciences and Engineering Research Council of Canada (NSERC) Industrial Research Chair Program, by the Canadian Institute for Photonic Innovations through the Packet-Switched Networks with Photonic Code-Based Processing Project, and by Québec's Regroupement Stratégique Center for Advanced Systems and Technologies in Communications. The work of B. J. Shastri was supported by NSERC through an Alexander Graham Bell Canada Graduate Scholarship and by McGill University through a Lorne Trottier Engineering Graduate Fellowship and McGill Engineering Doctoral Award.

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Digital Object Identifier 10.1109/JSTQE.2010.2041326

I. INTRODUCTION

DATA rates on fiber optic networks are increasing exponentially after having experienced constant growth for numerous decades. Fiber-to-the-premises/cabinet/building/home/user (FTTx) networks using single-mode fiber is capable of meeting these access network requirements at high (10+ Gb/s) data rates with superior network capacities. It is no longer a question of “if” FTTx is necessary to meet burgeoning residential and corporate user demands, it is a question of “when.” FTTx is therefore currently being aggressively deployed by the service-provider community worldwide [1], [2]. Passive optical networks (PONs) are an emerging multiaccess network technology based on all-optical core, and are recognized as the most promising solution for deploying FTTx [2]–[4]. PONs provide a low-cost solution to alleviate the so-called “last mile” problem that remains a bottleneck between the backbone network and high-speed local area networks (LANs). Consequently, the promise of a better bundle of distributive and interactive multimedia services such as video, voice, data, and fast Internet, to a large number of subscribers with guaranteed quality of service (QoS) by PONs, is compelling [5].

A PON typically has a physical tree topology with an optical line terminal (OLT) located at the root and optical network units (ONUs) connected to the branches. The existing PON standards, including the IEEE 802.3ah gigabit ethernet PON (GEPON) [6] and ITU-T G.984 gigabit-capable PON (GPON) [7], are based on time-division multiplexing (TDM), and can serve up to 32 or 64 users. Fig. 1 shows a general architecture of a standard commercial TDM-PON structure with our study in context. The maximum transmission distance between the ONUs and the OLT is usually 10–20 km. In the downstream direction, the network is point to point (P2P). Continuous data are broadcast from the OLT to the ONUs using TDM in the 1480–1550-nm wavelength band. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous-mode integrated circuits (ICs). The challenge in the design of a chip set for PONs comes from the upstream data path. In the upstream direction, the network is point to multipoint (P2MP); using time-division multiple access (TDMA), multiple ONUs transmit data in the 1310-nm window to the OLT in the central office (CO). To use the shared medium effectively, the ONUs require a burst-mode (BM) transmitter with a short turn-ON/OFF delay [8]. Because of optical path differences in the upstream path, packets can vary in amplitude ΔA and phase $\Delta\varphi$ —bursty data. The amplitude and phase of successive packets may vary anywhere between 0–20 dB and -2π to $+2\pi$ rad, respectively [9]. To deal with these

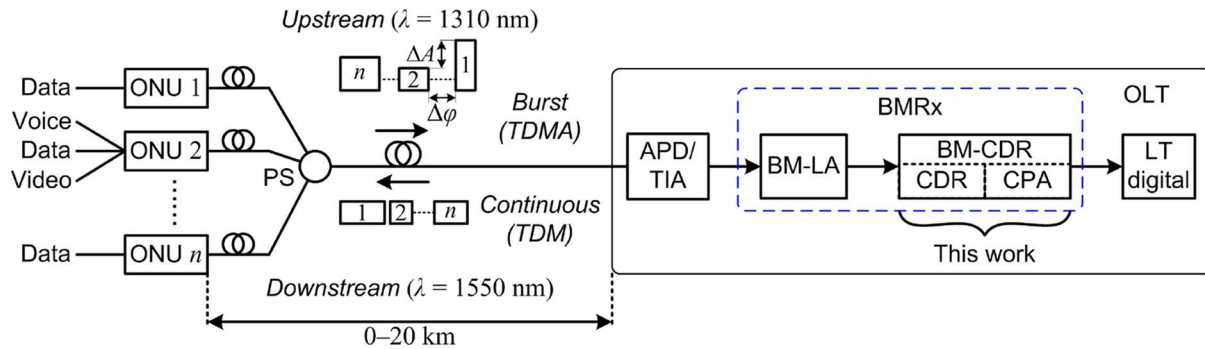


Fig. 1. Generic PON for FTTx showing our work on BM-CDR in context (APD: avalanche photodiode; BM-LA: burst-mode limiting amplifier; BMRx: burst-mode receiver; CDR: clock and data recovery; CPA: clock phase aligner; LT: line terminator; OLT: optical line terminal; ONU: optical network unit; TDM: time-division multiplexing; TIA: transimpedance amplifier; and TDMA: time-division multiple access).

variations, the OLT requires a BM receiver (BMRx). The BMRx is responsible for amplitude and phase recovery, which must be achieved at the beginning of every packet. At the front end of the BMRx is a BM limiting amplifier (BM-LA) responsible for amplitude recovery. Fast clock and data recovery (CDR) together with phase acquisition is then performed by a BM-CDR with the help of a clock phase aligner (CPA). The most important characteristic of the BM-CDR is its phase acquisition time, which must be as short as possible. This paper focuses on the BM-CDR aspect of the BMRx, both theoretically and experimentally.

A. Our Contributions

We briefly outline the two main contributions presented in this paper.

1) *Theoretical Modeling and Analysis*: We develop for the first time, to our knowledge, a unified probabilistic theory for: 1) conventional CDRs; 2) CDRs based on N times oversampling techniques in either time or space; 3) BM-CDRs built from oversampling CDRs. This theory can quantitatively explain the performance of these circuits in terms of the bit error rate (BER) and packet loss ratio (PLR). The model accounts for the following parameters: 1) silence period, including phase step and consecutive identical digits (CIDs), between consecutive packets; 2) frequency offset between the sampling clock and the data rate; 3) preamble length; 4) jitter on the sampling clock; and 5) pattern correlator error-resistance. Based on the theory, we perform a comprehensive theoretical analysis to assess the tradeoffs between these parameters, and compare the results experimentally to validate the theoretical model. This analysis coupled with the experimental results can be used to refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets.

2) *Novel 5 Gb/s BM-CDR*: In addition, we present a 5-Gb/s BM-CDR circuit based on an oversampling (in time) CDR operated at twice the bit rate and a CPA that makes use of a simple phase-picking algorithm for automatic clock phase acquisition. The end result is a BM-CDR with instantaneous phase acquisition and no trading-off in the loop bandwidth. Hence, the BM-CDR could also find applications in future high-speed optical burst/packet switched networks, which may require a cascade of BM-CDRs that each consumes some of

the overall jitter budget of the system. Instantaneous phase acquisition can be used as follows: 1) improve the physical efficiency of the upstream PON traffic; 2) reduce the BM sensitivity penalty; and 3) increase effective throughput of the system by increasing the information rate.

We also carry out a detailed set of experiments in a 20-km PON uplink to investigate the effect of silence period, including phase step and the length of CIDs, between successive upstream PON bursts from independent ONUs, received signal power, and finite frequency offset between the sampling clock and desired bit rate, on the BER and PLR performance of the BM-CDR. Consequently, we characterize the BM-CDR in terms of the phase acquisition time, CID immunity, BM sensitivity penalty, dynamic range, and frequency acquisition range.

B. Overview of the Paper

Following this introduction, the rest of the paper is organized as follows. In Section II, we summarize the current state of the art to lay the foundation for the research presented in this paper. Section III presents the architecture of the proposed BM-CDR and describe the phase-picking algorithm of the CPA. The unified probabilistic theory for CDRs (conventional and oversampling) and BM-CDRs is developed in Section IV. Based on this model, we present a detailed theoretical analysis in Section V. The design and implementation of the proposed BM-CDR is explained in Section VI. In Section VII, we describe the BM experimental setup, test signal specification, and measurement methodology used to test and characterize the BM-CDR in a 20-km PON uplink. Section VIII is devoted to the presentation and analysis of the experimental results. Finally, the paper is summarized and concluded in Section IX.

II. BACKGROUND

We briefly summarize the current state of the art along with its respective shortcomings. This will lay the foundation for the research presented in this paper. Within this context, our previously stated original contributions will become further apparent.

A. Probabilistic Theory of BM Receivers

Random noise, which is always present at the BMRx front end, affects the determination of the decision threshold and

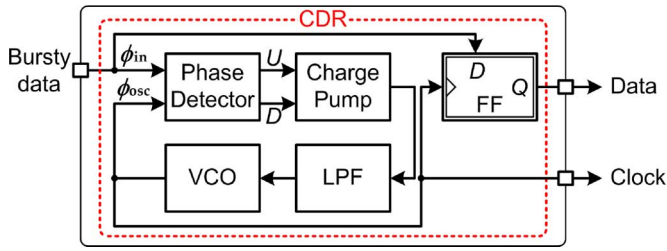


Fig. 2. Block diagram of a conventional CDR. (CDR: clock and data recovery; FF: flip-flop; LPF: low-pass filter; and VCO: voltage-controlled oscillator).

introduces sensitivity penalty. A sensitivity penalty that uses Gaussian noise statistics for BMRx using p-i-n photodiodes was first addressed in [10]. A more accurate model is provided in [11], while a unified theory that includes the interaction of Gaussian noise with the finite charging/discharging time of the adaptive threshold detection circuitry is derived in [9]. The influence of random dc offsets on the sensitivity of BMRx is analyzed in [12]. For BMRx employing avalanche photodiodes (APDs), where Gaussian approximation becomes unreliable, a sensitivity penalty analysis is detailed in [13]. Although there has been an appreciable amount of research on the theory of BMRx front-end circuits in literature, virtually no attention has been paid to the probabilistic theory of BM-CDRs.

B. Burst-Mode Clock and Data Recovery

1) *Problem of Clock Recovery*: PON systems employ a simple binary amplitude modulation data format—nonreturn to zero (NRZ)—for ease of detection. Random NRZ data have characteristic properties that directly influence the design of clock recovery circuits. The power spectral density (PSD), $S_{NRZ}(f)$, of an NRZ data sequence with normalized average power of unity is expressed as

$$S_{NRZ}(f) = \frac{T_b}{2} \left[\frac{\sin(\pi f T_b)}{\pi f T_b} \right]^2 \quad (1)$$

where f is the frequency parameter and T_b is the bit period. The spectrum of the NRZ data exhibits no spectral component (nulls) at integer multiples of the bit rate frequency $f = n/T_b$, $n = 1, 2, \dots$. This implies that a clock recovery circuit can lock to the spurious signals instead of the bit rate frequency or not at all. Furthermore, a linear time-invariant (LTI) operation cannot extract a periodic clock from these data [14]. However, the information about frequency of the data can be extracted from the spacing between the data transitions. These transitions appear as the rising and falling edges of the data signal. Thus, a nonlinear function, for example, edge detection with appropriate phase locking may be used to recover the clock. This is discussed next.

2) *BM Problem—Phase Acquisition*: Fig. 2 shows a block diagram of a conventional CDR circuit that senses data and produces a periodic clock. This phase-tracking CDR employs feedback to keep the recovered clock in phase with the clock embedded in the received data—a phase-locked loop (PLL). More specifically, the CDR is composed of a phase detector (PD), a

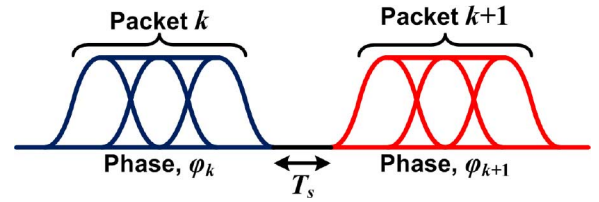


Fig. 3. Upstream PON traffic depicting the silence period between two successive bursts from independent ONUs.

charge-pump, a low-pass filter (LPF), a voltage-controlled oscillator (VCO), and a D flip-flop (FF). The PD is responsible for detecting the phase difference $\Delta\phi = \phi_{in} - \phi_{osc}$ between the center of the incoming data eye and the data-sampling clock. Depending on the phase difference, $\Delta\phi > 0$ rad (data leads clock) or $\Delta\phi < 0$ rad (data lags clock), the PD generates up (U) or down (D) signals respectively, for the charge pump. The charge pump then supplies the LPF with charge according to these signals. The filtered charge via the loop filter becomes the VCO control voltage, and either speeds up or slows down the clock, hence determining the frequency and phase of the sampling recovered clock. The generated clock signal is then used to drive the D-FF that retimes the data, i.e., it samples the noisy data, yielding an output with less jitter. As such, the D-FF is called a decision circuit. As the incoming data are regenerated, its additive noise and intersymbol interference (ISI) are suppressed while the amplitude is significantly amplified.

Under ideal conditions, with no ISI or clock jitter, error-free data recovery is achieved when the received data are sampled within half a bit period of the nominal sampling point. If the CDR is operated at the bit rate, the ideal sampling point is in the center of the data eye. In terms of the input clock phase ϕ_{in} and the recovered clock phase ϕ_{osc} , the condition for error-free data recovery is expressed as

$$|\phi_{in} - \phi_{osc}| < \pi \text{ rad}. \quad (2)$$

Fig. 3 depicts the silence period T_s between two successive bursts from independent ONUs, and can be expressed as

$$T_s = \left(m + \frac{\Delta\varphi}{2\pi} \right) T_b \quad (3)$$

where m , an all-zero sequence, is the number of CIDs and

$$|\Delta\varphi| = |\varphi_{k+1} - \varphi_k| \leq 2\pi \text{ rad} \quad (4)$$

representing the phase step that arises due to optical path differences between the consecutive k^{th} and $(k+1)^{\text{th}}$ packets. At the OLT, assuming that the CDR circuit is already in phase lock ($\Delta\phi = 0$ rad) by the end of the k^{th} packet, the resulting input phase step to the CDR by the arrival of the $(k+1)^{\text{th}}$ packet is given as

$$\phi_{in} = \Delta\varphi \cdot u(t), \quad \text{for } t > 0 \quad (5)$$

where

$$u(t) = \begin{cases} 0, & \text{if } t < 0 \\ 1, & \text{if } t > 0 \end{cases} \quad (6)$$

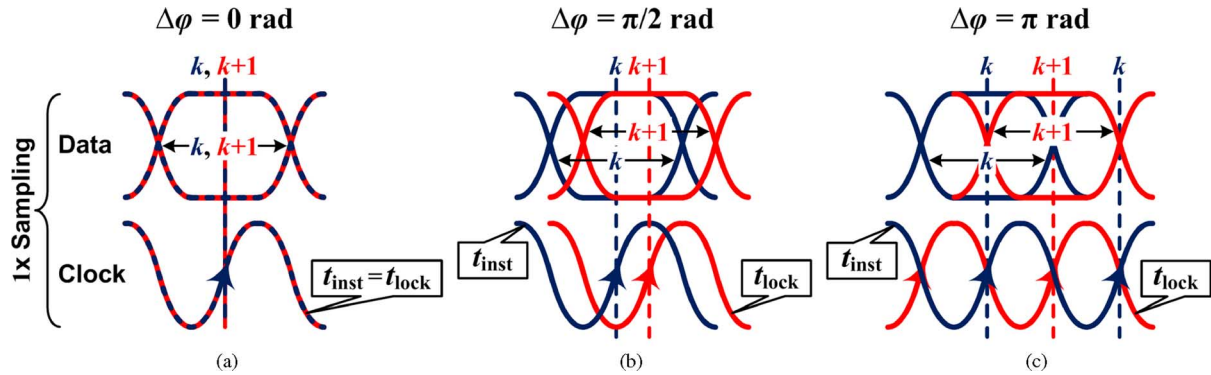


Fig. 4. Response of the conventional CDR to bursty traffic (consecutive packets with a phase step). Three different phase steps are considered: $\Delta\varphi = 0, \pi/2, \text{ and } \pi$ rad.

is a unit step function. Fig. 4 shows the response of the CDR to bursty traffic. The input phase step will result in the instantaneous clock t_{inst} , in-phase with the last bit of the k^{th} packet, to be out of phase by $|\Delta\varphi| \leq 2\pi$ rad with the first bit of the $(k+1)^{\text{th}}$ packet. This asynchronous and inevitable presence of phase steps between the received consecutive packets can cause conventional CDRs to lose pattern synchronization. Preamble bits l can be inserted at the beginning of each packet to allow the CDR feedback loop function,¹ $\eta(l) = \phi_{\text{osc}}/\phi_{\text{in}}$, enough time to settle down, and thus acquire lock, i.e., align the instantaneous clock t_{inst} , to the lock state t_{lock} , so as to sample in the middle of the data bit

$$\lim_{\eta(l) \rightarrow 1} t_{\text{inst}} = t_{\text{lock}}. \quad (7)$$

However, the use of a preamble introduces overhead, thus reducing the effective throughput and increasing delay. The most important characteristic of the BM-CDR is its phase acquisition time, which must be as short as possible to decrease the BM sensitivity penalty, and thus, increase the power budget or alternatively increase the information rate with more bits available to the packet payload. We define the lock acquisition time as the number of preamble bits l needed to achieve error-free operation. With the proposed BM-CDR, by sampling at twice the bit rate and employing the CPA discussed next, it will be demonstrated theoretically and experimentally that using the instantaneous clock t_{inst} , for sampling, suffices error-free data recovery for any phase step $|\Delta\varphi| \leq 2\pi$ rad between two consecutive packets. Hence, there is no need for a preamble field ($l = 0$), demonstrating instantaneous phase acquisition.

3) *BM Solution—Prior Art*: PONs have no repeaters in their data path unlike synchronous optical network (SONET) systems that impose a strict specification on jitter transfer. Jitter transfer refers to the suppression of the input jitter through the CDR circuit. Taking this into account, different approaches have been proposed to build BM-CDRs for PON applications by compromising the jitter transfer characteristics. These BM-CDRs are based on the follows: 1) broadband PLLs [15]; 2) injection-locking techniques [16]; 3) gated VCOs (GVCOs)

¹For a CDR based on a second order PLL, $\eta(l)$ is analytically expressed as (23).

TABLE I
BM-CDR SOLUTIONS BASED ON FEEDBACK, FEED-FORWARD, AND HYBRID ARCHITECTURES

Architecture	Solution	References
Feedback	Broad-band PLLs	[15]
	Injection locking	[16]
Feed-forward	Gated VCOs	[17]–[20]
	Blind-oversampling	[21], [22]
Hybrid	Semi-blind oversampling	This work and [23]

[17]–[20]; 4) oversampling CDRs without phase tracking—blind oversampling [21], [22]; and 5) hybrid combination of phase-tracking and blind-oversampling CDRs—semiblind oversampling [23]. These solutions broadly fall into three categories: 1) feedback architectures; 2) feedforward architectures; and 3) hybrid architectures—combination of feedback and feedforward. Table I classifies the current state-of-the-art BM-CDR solutions within these configurations.

Broadband PLLs-based BM-CDRs tradeoff the loop bandwidth of the PLL for fast phase acquisition time and large frequency capture range. The disadvantages include stability issues, jitter peaking, and limited jitter filtering. If additional control logic or a reset signal is acceptable, then a work around consists of using a dynamic-loop bandwidth; the bandwidth is increased while the CDR is acquiring lock and restored to its original value for the rest of the packet to minimize output jitter [24]. BM-CDRs based on injection-locking technique extracts the clock by injection, locking the local oscillator (LO) to the tiny embedded clock signal, which primarily arises from leakage coupling. This design suffers from severe performance degradation, as the natural frequency of the VCOs deviates from the data rate due to process, temperature, and supply variations (PVT). This consequently limits their frequency tracking range. BM-CDRs built from GVCO or some kind of gating circuit perform clock phase alignment by triggering a local clock on each transition of the input data. This solution provides rapid phase locking, but results in higher phase noise as it does not filter out input jitter. More seriously, the gating behavior would cause momentary fluctuation on the recovered clock, potentially incurring undesired jitter and ISI. In addition, the truncation or prolongation of the clock cycle during phase alignment induces other uncertainties such as locking (settling) time. The last

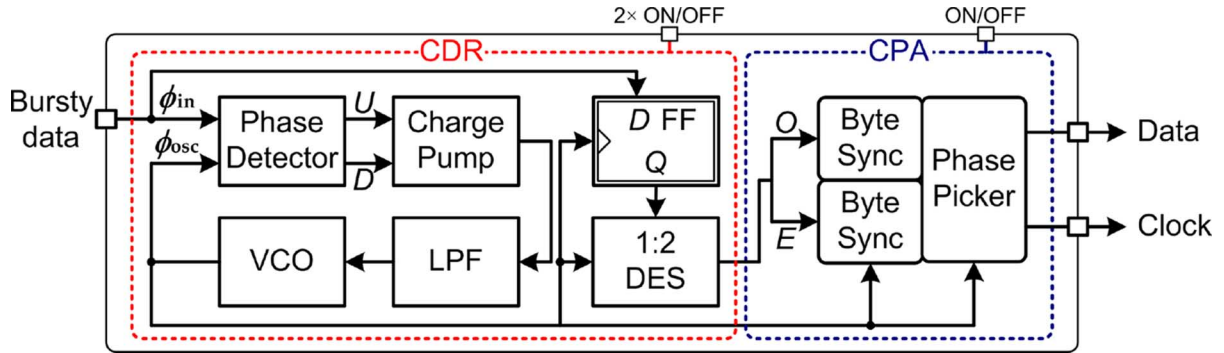


Fig. 5. Block diagram of the BM-CDR architecture based on a two-times semiblind oversampling CDR and CPA (CDR: clock and data recovery; CPA: clock phase aligner; DES: deserializer; FF: flip-flop; LPF: low-pass filter; Sync: synchronizer; and VCO: voltage-controlled oscillator).

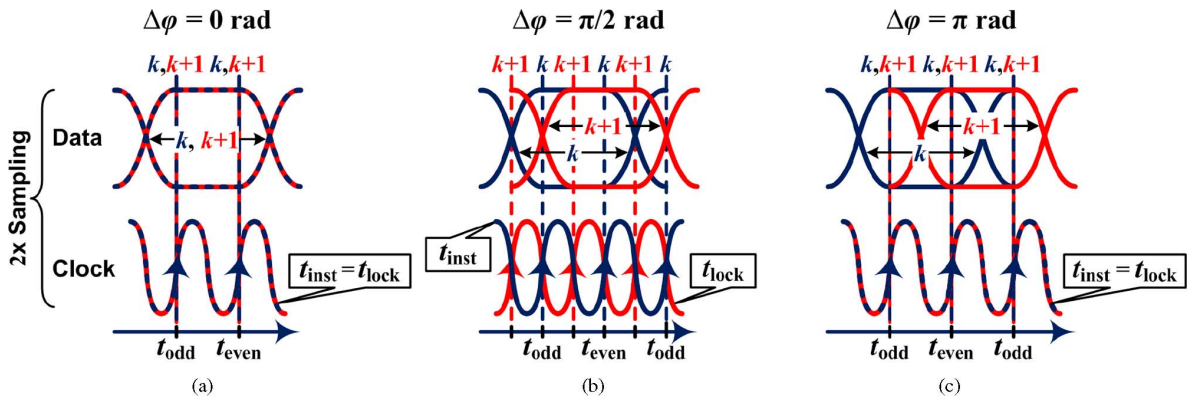


Fig. 6. Response of the two-times oversampling CDR to bursty traffic (consecutive packets with a phase step) with the depiction of the odd and even samples resulting from t_{odd} and t_{even} sampling instants. Three different phase steps are considered: $\Delta\varphi = 0, \pi/2,$ and π rad.

approach is based on oversampling without or with phase tracking, i.e., blind- or semiblind oversampling, respectively. One can either oversample in time using a clock frequency higher than the bit rate, or oversample in space using a multiphase clock with a frequency equal to the bit rate. Oversampling in time requires faster electronics, whereas oversampling in space requires low skew between multiple phases of the clock. The oversampling techniques, in general, suffer from high complexity and power consumption. The key advantage of the semiblind oversampling technique is that it produces a jitter tolerance, equal to the product of the phase-tracking jitter tolerance and the blind oversampling jitter tolerance, thereby increasing the low-frequency jitter tolerance. Note that jitter tolerance of the CDR refers to the peak-to-peak amplitude of sinusoidal jitter (as function of frequency) that can be applied at the input without causing data recovery errors. Our proposed BM-CDR is based on the semiblind oversampling² technique.

III. PROPOSED BM-CDR

A. Architecture

A block diagram of the proposed BM-CDR is shown in Fig. 5. The BM-CDR is composed of a phase-tracking CDR and a

CPA. The CDR can be operated in a two-times oversampling mode. Thus, the BM-CDR architecture, illustrated in Fig. 5, in essence can support three modes of operation: 1) conventional mode—a typical CDR; 2) oversampling mode—CDR operated at twice the bit rate; and 3) burst-mode—two-times oversampling CDR with the CPA. These modes of operation will be useful in measuring the relative performances theoretically and experimentally in the later sections.

1) *Clock and Data Recovery*: The operation of the CDR is as explained earlier. The key difference, however, is that the generated clock signal can be used to recover the received data by sampling the data twice per bit with the decision circuit. Fig. 6 shows the response of the CDR and the two-times oversampling CDR to bursty traffic. Recall that if the CDR is operated at the bit rate, the ideal sampling point is in the center of the data eye. In the case of a two-times oversampling CDR, the two sampling points of the recovered clock, t_{odd} and t_{even} , are located at $-\pi/2$ and $+\pi/2$ rad, respectively, from the center of the data bit. In terms of the input clock phase ϕ_{in} and the recovered clock phase ϕ_{osc} , the condition for error-free data recovery is expressed as

$$|\phi_{\text{in}} - \phi_{\text{osc}}| < \pi/2 \text{ rad.} \quad (8)$$

2) *Clock Phase Aligner*: As already mentioned, the BM functionality of the receiver is obtained by employing the CPA module. The CPA makes use of the two-times oversampling CDR and a simple, fast, and effective phase-picking algorithm

²For the sake of brevity, we will refer to semiblind oversampling as oversampling, unless otherwise explicitly stated. This is to differentiate it from blind oversampling.

[25], [26]. The odd and even samples (O and E , respectively, in Fig. 5) resulting from sampling the data twice on the alternate (t_{odd} and t_{even}) clock rising edges (two-times sampling in Fig. 6) are forwarded to path O and path E , respectively. The byte synchronizer is responsible for detecting the delimiter, which is a unique pattern indicating the start of the packet. It makes use of a payload detection algorithm to look for a preprogrammed delimiter pattern. Note that when there is no phase difference between the consecutive packets, $\Delta\varphi = 0$ rad, the odd and even samples are identical and uncorrupted. However, when there is a phase difference, $\Delta\varphi \neq 0$ rad, only one sample set is uncorrupted, while the other may or may not be corrupted. Then the concept behind the phase-picking algorithm is to replicate the byte synchronizer twice in an attempt to detect the delimiter on either the odd and/or even samples of the data, respectively. That is, regardless of any phase step $|\Delta\varphi| \leq 2\pi$ rad, there will be at least one clock edge (either t_{odd} or t_{even}) that will yield an accurate sample. The phase picker then uses feedback from the byte synchronizers to select the right path from the two possibilities. A more detailed explanation is presented in the next section.

B. Phase-Picking Algorithm—Intuitively

With the aid of some eye diagrams, we review the idea behind the phase-picking algorithm. Figs. 4 and 6 shows the response of the CDR operated at the bit rate and the two-times oversampling mode of the CDR with the CPA operation, respectively. Three specific phase differences between the consecutive packets are considered: 1) $\Delta\varphi = 0$ rad; 2) $\Delta\varphi = \pi/2$ rad; and 3) $\Delta\varphi = \pi$ rad. Note that although $\Delta\varphi = \pi$ rad represents a worst-case phase step for the CDR operated at the bit rate [see Fig. 4(c)], $\Delta\varphi = \pi/2$ rad phase step is the worst-case scenario for the oversampling CDR at twice the bit rate [see Fig. 6(b)]. The two-times oversampling mode produces two samples per bit, which helps the CPA algorithm to lock at the correct phase of the incoming packet. To understand how the CPA works, consider the case when there is no phase step ($\Delta\varphi = 0$ rad); path O correctly samples the incoming pattern [see t_{odd} in Fig. 6(a)]. For phase step $\Delta\varphi = \pi/2$ rad, path O will sample the bits on or close to the transitions after the phase step [see t_{odd} in Fig. 6(b)]. In this situation, the byte synchronizer of path O will likely not detect the delimiter at the beginning of the packet. On the other hand, the byte synchronizer of path E will have no problems detecting the delimiter [see t_{even} in Fig. 6(b)]. The phase picker controller monitors the state of the two byte synchronizers and selects the correct path accordingly (path E in this particular case). Once the selection is made, it cannot be overwritten until the comma is detected, indicating the end of the packet. This process repeats itself at the beginning of every packet. Similarly, for $\Delta\varphi = 3\pi/2$ rad phase step (not shown in Fig. 6 because the scenario is similar to the $\pi/2$ rad phase step), path E samples the bits on or close to the transitions, and thus, the phase picker controller selects path O . Consequently, the result is that the CPA achieves instantaneous phase acquisition (0 bit) for any phase step $|\Delta\varphi| \leq 2\pi$ rad, i.e., no preamble bits ($l = 0$) at the beginning of the packet are necessary. In the

next section, we provide a mathematical proof by deriving a theoretical probabilistic model for the BM-CDR.

IV. THEORETICAL MODELING

In this section, we develop a unified probabilistic theory for: 1) conventional CDRs; 2) CDRs based on N times oversampling techniques in either time or space; and 3) BM-CDRs built from oversampling CDRs. The theoretical model quantitatively explain the performance of these circuits in terms of the BER and PLR by taking into account the following parameters: 1) silence periods, including phase steps and the length of CIDs between successive upstream PON bursts from independent ONUs; 2) finite frequency offset between the sampling clock and desired bit rate; 3) preamble length; 4) jitter on the sampling clock; and 5) pattern correlator error resistance. Since all ONUs derive their timing information from the downstream OLT signal, we will assume that these circuits are already in frequency lock. In addition, we note that the model presented is for data transmitted in NRZ format, and it is independent of the bit rate and pulse shape, as long as the pulses are such that the ISI at the sampling point is negligible. This will remain valid at high bit rates, as long as the channel remains limited by Gaussian noise, and not by severe distortion of the eye diagram that results to closure at the sampling point [10]. It should also be noted that the model developed here represents the theoretical minimum and maximum bounds, and should not be confused with the performance of an actual circuit as it may vary depending on the implementation from one process or technology to another.

A. Framework

Jitter can be interpreted as the perturbations of the threshold crossing time of data transitions from their ideal position in time. Jitter affects the overall quality of the signal at the receiver in three ways [27]: 1) stability of the rise and fall times of the data bits; 2) stability of the rise and fall slopes of the data bits; and 3) stability of the width of the data bits. A part of the jitter of the data is inherited as phase uncertainty of the recovered sampling clock in the clock recovery circuit. As a result, the regenerated (retimed) data sequence by the CDR may be erroneous, degrading the BER and PLR performance. Jitter is, in general, classified into two main categories, namely, random jitter and deterministic jitter.

Random jitter (RJ) is unpredictable, unbounded, and results from physical noise sources based on random processes. The most prevalent RJ mechanism is thermal noise; however, other causes include shot noise and flicker ($1/f$) noise. The generation of RJ is approximated to a Gaussian probability distribution. This follows from the central limit theorem, which states that composite effect of many uncorrelated noise sources, regardless of the distributions, approaches a Gaussian distribution. The Gaussian approximation [28] is sufficiently accurate for design purposes and far easier to evaluate than the more exact probability distribution within the receiver [29]. RJ is characterized by the standard deviation or the rms value of the Gaussian probability distribution.

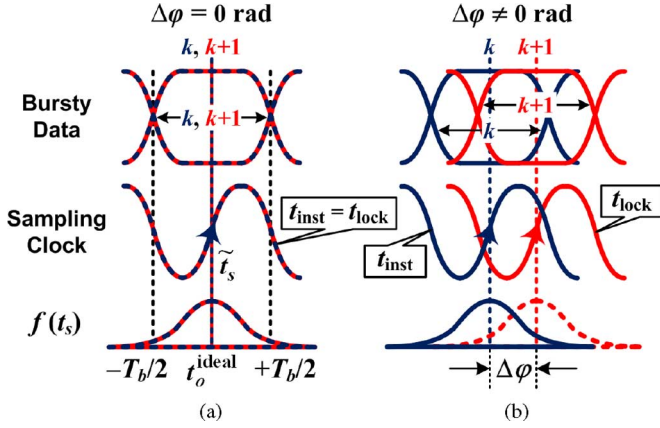


Fig. 7. Graphical depiction of the actual clock sampling point \tilde{t}_s , in the presence of random jitter, and the associated probability density function $f(t_s)$, when the phase difference: (a) $\Delta\varphi = 0$ rad and (b) $\Delta\varphi \neq 0$ rad.

Deterministic jitter (DJ) is predictable, bounded, and attributed to several causes such as duty cycle distortions (DCDs), and initial frequency offset (when a clock from free running tries to lock in a reference clock). This type of jitter, being deterministic and not random, cannot be described by distributions. DJ is further classified as ISI and data-dependent jitter (DDJ), pulsewidth-distortion jitter (PWDJ), sinusoidal jitter (SJ), and uncorrelated bounded jitter (UBJ). The effect of DJ is to shrink the data eye by a finite amount, and will only further deteriorate the performance of the CDR and the BM-CDR. Thus, in order to simplify the derivation of the theoretical models and the corresponding theoretical analysis, DJ is ignored.

In deriving the theoretical probabilistic model, we make use of continuous random variables \tilde{x} , which follow a Gaussian distribution denoted as $\tilde{x} \sim N(\mu, \sigma^2)$, where μ is the mean, $\sigma > 0$ is the standard deviation, and the probability density function (PDF) $f(x)$ of \tilde{x} is given by

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right), \quad x \in \mathbb{R} \quad (9)$$

with the following characteristics: $f(x) > 0$, for all x , and $\int_{-\infty}^{+\infty} f(x)dx = 1$.

B. BER Probability Model

In the context of CDR, we define the following continuous random variables with a Gaussian distribution.

- 1) $\xi \sim N(0, \sigma_{\xi}^2)$, with PDF $f(\xi)$, is the jitter on the edges of the data bits with a zero mean, where σ_{ξ} corresponds to the rms jitter on the sampling clock signal.
- 2) $\tilde{t}_s \sim N(\tilde{t}_o, \sigma_{\tilde{t}_s}^2)$, with PDF $f(t_s)$, is the actual clock sampling point in the presence of random jitter.
- 3) $\tilde{t}_o \sim N(t_o^{\text{ideal}}, \sigma_{\tilde{t}_o}^2)$, with PDF $f(t_o)$, is the clock sampling point determined by the CDR, where t_o^{ideal} is the ideal clock sampling point in the middle of the data bit and $\sigma_{\tilde{t}_o}^2 = \kappa\sigma_{\tilde{t}_s}^2$, with κ being a constant of proportionality.

For convenience, the left and right edges of the data eye are located at $-T_b/2$ and $+T_b/2$, respectively, as portrayed in Fig. 7(a). Thus, the expectation (mean) of the clock sampling

point is given by

$$E[\tilde{t}_o] \triangleq \int_{-\infty}^{+\infty} t_o f(t_o) dt_o = t_o^{\text{ideal}} = 0 \quad (10)$$

as the ideal clock sampling point is in the center of the data bit. Let $\tilde{\xi}_j^{\text{left}}$ and $\tilde{\xi}_j^{\text{right}}$ be the jitter on the left edge and right edge of the j^{th} bit of an l -bit preamble. We assume that $\tilde{\xi}_j^{\text{left}}$ and $\tilde{\xi}_j^{\text{right}}$ are independent with common rms jitter σ_{ξ} . Then the midpoint of the j^{th} bit $\tilde{\tau}_j$ is expressed as

$$\tilde{\tau}_j = \frac{\tilde{\xi}_j^{\text{left}} + \tilde{\xi}_j^{\text{right}}}{2}. \quad (11)$$

After the l -bit preamble, the clock sampling point determined by the CDR \tilde{t}_o , at the first bit where the decision circuit will start sampling the data bits, is given by the average of the individual midpoints in (11) as

$$\tilde{t}_o = \frac{1}{(l+1)} \sum_{j=1}^{l+1} \tilde{\tau}_j. \quad (12)$$

Subsequently, $\sigma_{\tilde{t}_o}$ can be related to the sampling clock rms jitter $\sigma_{\tilde{t}_s}$ as follows:

$$\begin{aligned} \sigma_{\tilde{t}_o}^2 &\triangleq E\left[\left(\tilde{t}_o - \underbrace{E[\tilde{t}_o]}_{=0}\right)^2\right] = E\left[\left(\frac{1}{(l+1)} \sum_{j=1}^{l+1} \tilde{\tau}_j\right)^2\right] \\ &= \frac{1}{4(l+1)^2} \left\{ \sum_{j=0}^l \underbrace{\left(E\left[\left(\tilde{\xi}_j^{\text{left}}\right)^2\right]\right)}_{=\sigma_{\xi}^2} + E\left[\left(\tilde{\xi}_j^{\text{right}}\right)^2\right]}_{=\sigma_{\xi}^2} \right. \\ &\quad \left. + 2 \underbrace{E\left[\tilde{\xi}_j^{\text{left}} \cdot \tilde{\xi}_j^{\text{right}}\right]}_{=0(\text{uncorrelated})} \right\} \\ &= \underbrace{\frac{1}{2(l+1)}}_{=\kappa} \sigma_{\tilde{t}_s}^2. \end{aligned} \quad (13)$$

Hence, the PDFs of the actual clock sampling point $f(t_s)$ and the clock sampling point determined by the CDR $f(t_o)$ can be expressed as follows:

$$f(t_s) = \frac{1}{\sqrt{2\pi} \cdot \sigma_{\tilde{t}_s}} \exp\left(-\frac{(t_s - \tilde{t}_o)^2}{2\sigma_{\tilde{t}_s}^2}\right) \quad (14)$$

$$f(t_o) = \frac{1}{\sigma_{\tilde{t}_o}} \sqrt{\frac{(l+1)}{\pi}} \exp\left(-\frac{(l+1)t_o^2}{\sigma_{\tilde{t}_o}^2}\right). \quad (15)$$

The probability that the clock sampling point determined by the CDR \tilde{t}_o will be within the data bit after l preamble bit is given by

$$\begin{aligned} \Pr\left(|\tilde{t}_o| < \frac{T_b}{2}\right) &= \int_{-T_b/2}^{+T_b/2} f(t_o) dt_o \\ &= 1 - 2Q\left(\frac{1}{\sigma_{\tilde{t}_o} [\text{UI}]} \sqrt{\frac{(l+1)}{2}}\right) \end{aligned} \quad (16)$$

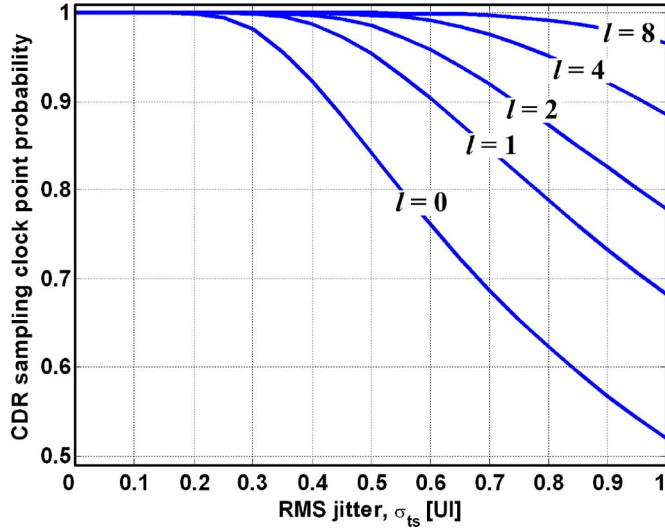


Fig. 8. Probability of the clock sampling point determined by the CDR \tilde{t}_o to be within the data bit after an l -bit preamble.

where $Q(\cdot)$, called the “ Q function,” is the normalized Gaussian-tail probability defined as

$$Q(x) \triangleq \frac{1}{\sqrt{2\pi}} \int_x^{\infty} \exp\left(-\frac{\lambda^2}{2}\right) d\lambda. \quad (17)$$

Note that (16) has been made independent of the data rate. Thus, the rms jitter σ_{t_s} is expressed in terms of the unit interval (UI); 1 UI corresponds to a 1-bit period T_b . In Fig. 8, we plot (16) as a function of the rms jitter σ_{t_s} for different preamble lengths. It can be observed that the probability $\Pr(|\tilde{t}_o| < T_b/2)$ decreases with increasing jitter, but can be compensated by increasing the preamble length. Also, for $\sigma_{t_s} \leq 0.25$ UI, $\Pr(|\tilde{t}_o| < T_b/2) \sim 1$ even with no preamble bits.

When there is no phase difference, $\Delta\varphi = 0$ rad, between two consecutive packets in a PON uplink, as depicted in Fig. 7(a), the CDR’s sampling error probability is equivalent to the probability that the clock transition occurs either before the leading data transition or after the trailing data transition, $\Pr(|\tilde{t}_s| > T_b/2)$, given that the sampling point determined by the CDR \tilde{t}_o is within the data eye. Assuming uncorrelated data with equiprobable 1’s and 0’s, the sampling error probability P_s of the CDR can be expressed as

$$P_s = \frac{1}{2} \Pr\left(|\tilde{t}_o| < \frac{T_b}{2}\right) \Pr\left(|\tilde{t}_s| \geq \frac{T_b}{2}\right) \quad (18)$$

where

$$\Pr\left(|\tilde{t}_s| \geq \frac{T_b}{2}\right) = \int_{-\infty}^{-T_b/2} f(t_s) dt_s + \int_{+T_b/2}^{+\infty} f(t_s) dt_s. \quad (19)$$

Ideally, the sampling clock must bear a well-defined phase relationship with respect to the received data, so that the decision circuit samples each bit at the midpoint of the data eye.

Thus, it is desirable that the CDR clock sampling point be as close as possible to the ideal clock sampling point, i.e., $\tilde{t}_o \sim t_o^{\text{ideal}} = 0$. Also, since the PDF $f(t_s)$ is even symmetric, then $\Pr(\tilde{t}_s < -T_b/2) = \Pr(\tilde{t}_s > +T_b/2)$, and the sampling error probability is given as

$$P_s = Q\left(\frac{T_b}{2\sigma_{t_s}}\right). \quad (20)$$

1) Finite Phase Step Consideration: With a finite phase difference, i.e., $\Delta\varphi \neq 0$ rad, between the consecutive packets, as illustrated in Fig. 7(b), the phase step has the effect of displacing the instantaneous sampling clock determined by the CDR t_{inst} by $|\Delta\varphi|(T_b/2\pi)$. By inserting preamble bits, the CDR feedback loop will have time to settle down. Specifically, after an l -bit preamble, the clock sampling point determined by the CDR \tilde{t}_o will be displaced by $t_{|\Delta\varphi|} = |\Delta\varphi|(1 - \eta(l))(T_b/2\pi)$, where $\eta(l) = \phi_{\text{osc}}/\phi_{\text{in}}$ is the response of the PLL to an input phase step $\phi_{\text{in}} = \Delta\varphi u(t)$, for $t > 0$, with $u(t)$ being the unit step function in (6), and ϕ_{osc} is the phase of the recovered sampling clock (see Fig. 5). Note that the expression for $t_{|\Delta\varphi|}$ is only valid for phase steps $|\Delta\varphi| \leq \pi$ rad and does not account for $\pi < |\Delta\varphi| \leq 2\pi$ rad. Thus, a correcting factor ψ must be introduced to account for the symmetrical performance about the edges of the data bit at $-T_b/2$ and $+T_b/2$. Hence, the displacement $t_{|\Delta\varphi|}$ of the clock sampling point determined by the CDR \tilde{t}_o , after an l -bit preamble can be expressed as

$$t_{|\Delta\varphi|} = \left[(|\Delta\varphi| - \psi)(1 - \eta(l)) \right] \frac{T_b}{2\pi} \quad (21)$$

where

$$\psi = \begin{cases} 0, & \text{if } |\Delta\varphi| \leq \pi \text{ rad} \\ 2\pi, & \text{if } \pi < |\Delta\varphi| \leq 2\pi \text{ rad.} \end{cases} \quad (22)$$

For a CDR based on a second-order PLL, $\eta(l)$ is analytically derived to be [30]

$$\eta(l) = 1 - \exp(-l\zeta\omega_n T_b) \times \left\{ \cosh\left(l\omega_n T_b \sqrt{\zeta^2 - 1}\right) - \frac{\zeta}{\sqrt{\zeta^2 - 1}} \sinh\left(l\omega_n T_b \sqrt{\zeta^2 - 1}\right) \right\}, \quad \text{for } \zeta > 0 \quad (23)$$

where ζ is the “damping ratio” and ω_n (in radians per second) is the “natural frequency,” both being functions of the CDR circuit parameters: charge-pump current, capacitance of the LPF, gain of the VCO, and data transition density [14].

It follows from (21) that the PDF $f(t_s)$ in (14) can therefore be modified to account for this phase step as

$$f(t_s) = \frac{1}{\sqrt{2\pi}\sigma_{t_s}} \exp\left(-\frac{(t_s - \tilde{t}_o \mp t_{|\Delta\varphi|})^2}{2\sigma_{t_s}^2}\right). \quad (24)$$

Thus, the probability that the clock transition occurs either before the leading data transition or after the trailing data transition

can then be expressed as

$$\Pr\left(|\tilde{t}_s| \geq \frac{T_b}{2}\right) = \frac{1}{2} \left\{ Q\left(\frac{\frac{T_b}{2} - \tilde{t}_o - t_{|\Delta\varphi|}}{\sigma_{t_s}}\right) + Q\left(\frac{\frac{T_b}{2} - \tilde{t}_o + t_{|\Delta\varphi|}}{\sigma_{t_s}}\right) \right\}. \quad (25)$$

Before we proceed, we make two assumptions: 1) the clock sampling point determined by the CDR is ideally located at the center of the data eye ($\tilde{t}_o = 0$) *before* a phase step $|\Delta\varphi|$ and 2) the rms jitter on the clock signal $\sigma_{t_s} \leq 0.25$ UI, implying the probability that the CDR clock sampling point is within the data eye *after* the phase step is $\Pr(|\tilde{t}_o| < T_b/2) \sim 1$, for any number of preamble bits l . Consequently, for a given phase step $|\Delta\varphi| \leq 2\pi$ rad, the sampling error probability P_s in (18) can be expressed as

$$P_s(|\Delta\varphi|) = \frac{1}{2} \cdot \left\{ Q\left(\frac{\pi - (|\Delta\varphi| - \psi)(1 - \eta(l))}{2\pi\sigma_{t_s}[\text{UI}]}\right) + Q\left(\frac{\pi + (|\Delta\varphi| - \psi)(1 - \eta(l))}{2\pi\sigma_{t_s}[\text{UI}]}\right) \right\}. \quad (26)$$

For a CDR that is based on an N times oversampling architecture in either time or space, the absolute value of the maximum phase difference between the ideal sampling point and the sampling point determined by the CDR is $\max(|t_o^{\text{ideal}} - \tilde{t}_o|) = T_b/2N \equiv \pi/N$ rad. For $t_o^{\text{ideal}} = 0$, the N -clock sampling points determined by the CDR $t_o^n|_N$ are located at

$$\tilde{t}_o \in \{t_o^n|_N\} = \left\{ \frac{\pi}{N}(2n + 1 - N) \right\} \quad (27)$$

for $n = 0, 1, \dots, N - 1$. For each of the N data samples, the sampling error probabilities $P_s^n|_N$ can be calculated by convolving $P_s(|\Delta\varphi|)$ in (26), with the N sampling points $t_o^n|_N$ in (27), as

$$P_s^n|_N = P_s(|\Delta\varphi|) \otimes \delta(|\Delta\varphi| - t_o^n|_N) \quad (28)$$

where

$$\delta(|\Delta\varphi| - t_o^n|_N) \triangleq \begin{cases} 1, & \text{if } |\Delta\varphi| = t_o^n|_N \\ 0, & \text{if } |\Delta\varphi| \neq t_o^n|_N \end{cases} \quad (29)$$

is the Dirac-delta function. It follows from the sifting property

$$\begin{aligned} P_s^n|_N &= \int_{-\infty}^{+\infty} P_s(|\Delta\varphi| - \lambda) \delta(\lambda - t_o^n|_N) d\lambda \\ &= P_s(|\Delta\varphi| - t_o^n|_N). \end{aligned} \quad (30)$$

The sampling error probability $P_s^{2\times\text{-CDR}}$ for a two-times oversampling CDR is given by the sample set

$$P_s^{2\times\text{-CDR}} = \{P_s^{\text{odd}}, P_s^{\text{even}}\} \quad (31)$$

where

$$P_s^k = P_s(|\Delta\varphi| - t_k), \quad \text{for } t_k = \begin{cases} -\pi/2 \text{ rad}, & \text{if } k \equiv \text{odd} \\ +\pi/2 \text{ rad}, & \text{if } k \equiv \text{even} \end{cases} \quad (32)$$

with t_k being the odd and even clock sampling points determined by the CDR obtained from (27) for $N = 2$. Consequently, for a BM-CDR based on the two-times oversampling CDR and a CPA, which selects the correct set of samples (odd or even) with the aid of a phase-picking algorithm (see Section III-B), the sampling error probability $P_s^{\text{BM-CDR}}$ is given by

$$P_s^{\text{BM-CDR}} = \min\{P_s^{\text{odd}}, P_s^{\text{even}}\}. \quad (33)$$

We define the BER, denoted as P_e , of the CDR, two-times oversampling CDR, and BM-CDR, from the sampling error probabilities in (26), (31), and (33) as follows:

$$\text{BER} \equiv P_e \triangleq \begin{cases} P_s(|\Delta\varphi|), & \text{for CDR} \\ \{P_s^{\text{odd}}, P_s^{\text{even}}\}, & \text{for two-times CDR} \\ \min\{P_s^{\text{odd}}, P_s^{\text{even}}\}, & \text{for BM-CDR.} \end{cases} \quad (34)$$

2) *Finite Frequency Offset Consideration*: Recall from (3) that the silence period T_s , between two consecutive bursts from independent ONUs, consists, in addition to a phase step, of an all-zero sequence of m CIDs. The presence of CIDs can cause the frequency of the LO, usually implemented as a crystal, to inevitably drift from the desired bit rate by a few tens of parts per million (PPM), such that the recovery of data would no longer be possible. The frequency error thus accumulates during consecutive runs of 1's or 0's, resulting to jitter in the time domain. To quantify jitter, frequency deviation Δf is defined as [31]

$$\Delta f = f_b - K f_{\text{ref}} \quad (35)$$

where $f_b = 1/T_b$ is the data rate, f_{ref} is the reference frequency, and K is the corresponding divide ratio. Since Δf is typically less than f_b , the sampling clock zero crossing shifts by $\Delta f/f_b$ per bit period during long runs [31]. For m CIDs, the phase error $\Delta\varphi_e$ between two consecutive bursts can accumulate up to

$$\Delta\varphi_e = 2\pi k(m - 1) \frac{\Delta f}{f_b} \quad (36)$$

in the last bit. This is, of course, an optimistic estimation since the noise, in particular VCO phase noise, would deteriorate the result considerably. For a CDR that uses both the rising *and* falling edges of the input data to adjust the clock phase, $k = 1$; in the case where the CDR uses only the rising *or* falling edge of the data input, $k = 2$ [17]. In the worst case when the phase error $|\Delta\varphi_e|$ exceeds π rad, the maximum tolerable length of CIDs m_{max} in the presence of frequency offset is given by

$$m_{\text{max}} = \frac{1}{2k} \left| \frac{f_b}{\Delta f} \right| + 1. \quad (37)$$

The rms jitter on the sampling clock due to this effect can be derived to be [31]

$$\sigma_{t_s} = \sqrt{2} \left| \frac{\Delta f}{f_b} \right|. \quad (38)$$

C. PLR Probability Model

We now theoretically relate the PLR performance of the receiver to the BER performance. The BER will affect the bits in the packet delimiter. If the delimiter is not being correctly detected, the packet is declared lost, hence contributing to the packet loss count. The error resistance of the delimiter depends not only on its length, but also on the exact implementation of the pattern correlator. Let P_l^z represent the PLR obtained at a given BER of P_e with a pattern correlator having an error resistance of z bits in a d -bit delimiter. The PLR can then be estimated as

$$\text{PLR} \equiv P_{l_z} \leq \sum_{j=z+1}^d \Pr(j) \sim \Pr(z+1), \quad \text{for } P_e \ll 1 \quad (39)$$

where $\Pr(x)$ gives the probability of finding x errors out of a d -bit delimiter, given that the probability of finding a bit error is P_e , and can be expressed as a binomial distribution as

$$\Pr(x) = \binom{d}{x} P_e^x (1 - P_e)^{d-x}. \quad (40)$$

V. THEORETICAL ANALYSIS

On the basis of the theoretical probabilistic model developed in Section IV, we quantitatively analyze the performance of the proposed BM-CDR in Section III. More specifically, we investigate the BER and PLR performance of the BM-CDR by assessing the tradeoffs between the following parameters: 1) silence period, including phase step and length of CIDs, between consecutive packets from independent ONUs; 2) preamble length; 3) rms jitter on the recovered sampling clock; 4) pattern correlator error resistance; and 5) finite frequency offset between the LO and the desired bit rate.

A. Effect of Phase Step

The plots shown in Fig. 9 show the performance of a conventional CDR, two-times oversampling CDR, and BM-CDR (two-times oversampling CDR and CPA), in terms of the BER P_e in (34) and PLR P_{l_z} in (39), as a function of phase step $|\Delta\phi| \leq 2\pi$ rad. Note that in all three figures, the preamble length $l = 0$, rms jitter on the recovered sampling clock $\sigma_{t_s} = 0.02$ UI, and pattern correlator error resistance $z = 0$. As shown in Fig. 9(a) the worst-case phase steps for the CDR are $\Delta\phi = \pm\pi$ rad because these represent the half-bit periods, and therefore, the CDR is sampling exactly at the transition of the eye diagram, resulting to a BER ~ 0.5 and a PLR ~ 1 . This is as expected from the explanation provided in Section III-B [see Fig. 4(c)]. At phase shifts (near) $\Delta\phi \in \{0 \text{ rad}, \pm 2\pi \text{ rad}\}$, we can easily achieve error-free operation, $\text{BER} < 10^{-10}$ and $\text{PLR} < 10^{-6}$, because the CDR is almost sampling at the middle of each data bit. For the two-times oversampling mode depicted in Fig. 9(b), the worst-case phase steps $\Delta\phi \in \{\pm\pi/2 \text{ rad}, \pm 3\pi/2 \text{ rad}\}$ result from sampling the data on either the odd and/or even clock rising edges [see Fig. 6(b)]. It should be noted that although $\Delta\phi = \pm\pi$ rad phase steps represent the worst-case scenario for the conventional CDR, a two-times oversampling CDR does not

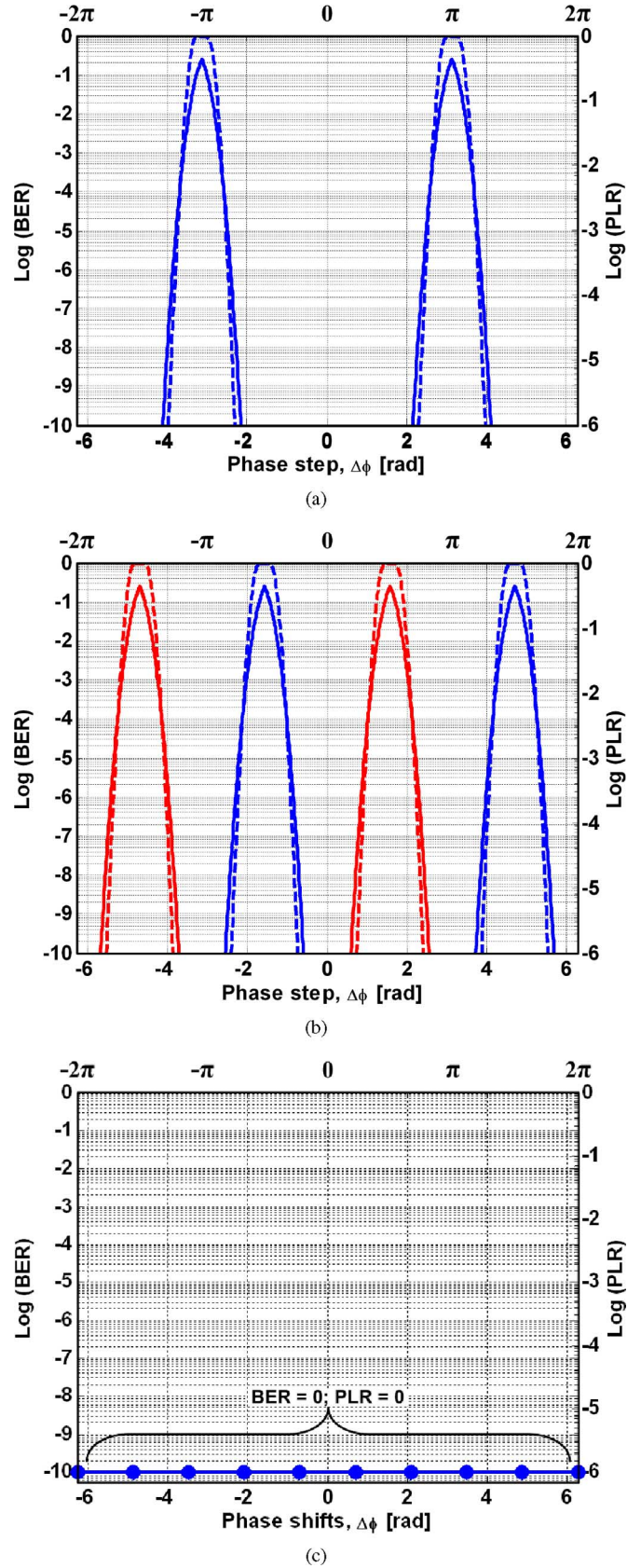


Fig. 9. BER and PLR performance versus phase step for a zero preamble length (solid lines for BER curves; dashed lines for PLR curves). (a) Conventional CDR. (b) Two-times oversampling CDR. (c) BM-CDR (two-times oversampling CDR + CPA).

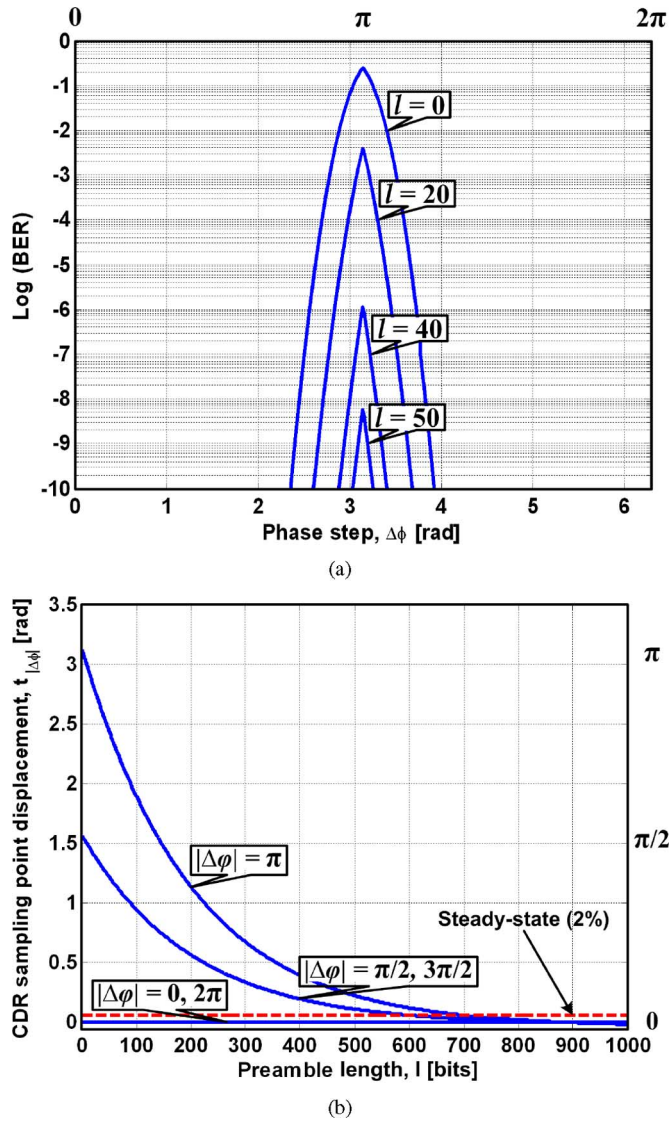


Fig. 10. Comparison of two methodologies for measuring the phase acquisition time. (a) BER performance versus phase step and preamble length. (b) CDR sampling point displacement versus phase step and preamble length.

need to realign the sampling clock in such cases [see Fig. 6(c)]. Finally, for the BM-CDR performance shown in Fig. 9(c), we achieve error-free operation for any phase step $|\Delta\phi| \leq 2\pi$ rad. The progression from Fig. 9(a)–(c) shows that two-times oversampling, combined with the appropriate CPA, can turn a conventional CDR into a BM-CDR with instantaneous phase acquisition (0 bit), thus verifying the claim made in Section III.

B. Effect of Preamble length

In order to compare the performance of the BM-CDR to the phase acquisition time of the conventional CDR, consider the plot shown in Fig. 10(a), which illustrates the BER performance of the CDR as a function of phase step. We have restricted the horizontal axis to values from $0 \leq \Delta\phi \leq 2\pi$ rad as the results are symmetrical about 0 rad from $-2\pi \leq \Delta\phi \leq 0$ rad. Also note that, for convenience only, the BER performance has been

shown. We measure the phase acquisition time of the CDR by increasing the length of the preamble until error-free operation is achieved. Preamble bits (“1010...”) pattern are inserted at the beginning of the packet to help the PLL of the CDR to settle down and acquire lock. As the preamble length is increased, the BER for the worst-case phase step $|\Delta\phi| = \pi$ rad improves as the maximum (upper bound) of the curve decreases, and for a given BER, the phase step range for inducing errors becomes smaller as the curve narrows. After 50 preamble bits, we observe error-free operation for any phase step. However, the use of the preamble reduces the effective throughput and increases delay.

Before concluding this section, it should be noted that this method of measuring the phase acquisition time is more accurate than the qualitative method of monitoring the setting time of the CDR’s sampling clock to within a certain percentage (usually 2%–5%) of the steady-state value, as shown in Fig. 10(b) where we plot (21). The drawback of the latter method is that it overestimates the lock acquisition time—a 14-fold discrepancy. This is because it is not necessary for the sampling clock to be perfectly in the middle of the data bit during the data recovery, but only close enough depending on the rms jitter on the sampling clock. The effect of rms jitter will be discussed next. We therefore conclude that the settling time provides, at best, a relative measure of the phase acquisition time.

C. Effect of rms Jitter

Here, we examine the effect that the rms jitter on the recovered sampling clock has on the performance of the CDR and the BM-CDR in terms of the phase acquisition time and the BER. In Fig. 11(a), we plot the maximum allowable rms jitter so as to maintain a $\text{BER} \leq 10^{-10}$ as a function of phase step for different preamble lengths. It can be observed that this dependence is linear and symmetrical about the worst-case phase step at $|\Delta\phi| = \pi$ rad. For phase steps $\Delta\phi \in \{0 \text{ rad}, \pm 2\pi \text{ rad}\}$, the maximum allowable jitter $\sigma_{t_s}^{\text{max}} = 0.08$ UI for any preamble length; however, at $|\Delta\phi| = \pi$ rad, $\sigma_{t_s}^{\text{max}} = 0$ UI for no preamble bits $l = 0$. This implies that it is not feasible for the CDR to obtain instantaneous phase acquisition since a jitter-free sampling clock is practically impossible. With increasing preamble length, the jitter tolerance on the sampling clock increases for a given phase step, and tends to become independent of the phase step in the presence of a large number of preamble bits:

$$\lim_{l \rightarrow \infty} \sigma_{t_s}^{\text{max}} = 0.08 \text{ UI, for all } |\Delta\phi| \leq 2\pi \text{ rad.} \quad (41)$$

To compare the performance of the CDR with the BM-CDR, examine the plots shown in Fig. 11(b), which show the number of preamble bits required to obtain a $\text{BER} \leq 10^{-10}$ as a function of the rms jitter for the worst-case phase step $|\Delta\phi| = \pi$ rad. The proposed BM-CDR is able to achieve instantaneous phase acquisition when the rms jitter $\sigma_{t_s} \leq 0.02$ UI. This is true for any phase step $|\Delta\phi| \leq 2\pi$ rad, as shown in Fig. 9(c). It is interesting to note that in the case of the CDR, a jitter tolerance of 0.02 UI corresponds to a preamble length of more than 50 bits for $|\Delta\phi| = \pi$ rad. This confirms our findings in Fig. 10(a) and, in particular, the measurement methodology.

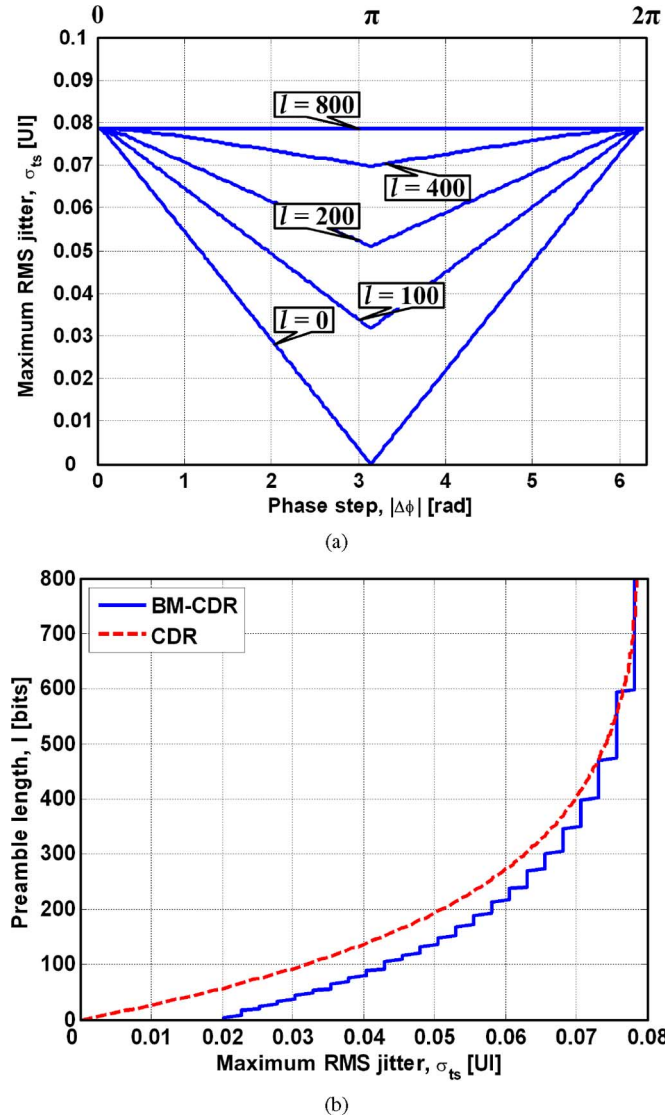


Fig. 11. (a) Maximum allowable rms jitter on the CDR sampling clock versus phase step and preamble length to maintain a $\text{BER} \leq 10^{-10}$. (b) Comparison with BM-CDR; preamble length versus rms jitter to achieve a $\text{BER} \leq 10^{-10}$ for the worst-case phase step $|\Delta\phi| = \pi$ rad.

In addition, in Fig. 12, we plot the BER performance of the CDR and the BM-CDR as a function of the rms jitter for different phase steps and zero preamble bits. As anticipated, for a given BER and phase step, the allowable rms jitter is higher with the BM-CDR than with the CDR in each case. More importantly, it can be perceived that the BM-CDR achieves far superior BERs for any given phase step and rms jitter.

D. Effect of Pattern Correlator Error Resistance

To improve the system performance, forward-error correcting (FEC) schemes can be employed by encoding the packet bits. Due to the associated overhead, most standards impose a strict requirement on the delimiter field—a unique pattern of fixed length. Therefore, while the payload bits can be encoded, it is usually not possible to encode the delimiter bits. Hence, although there is an improvement in the BER performance at a

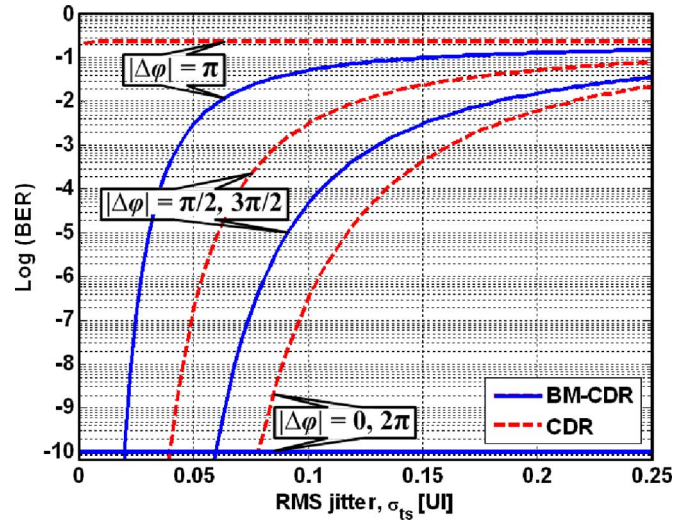


Fig. 12. BER performance of the CDR and the BM-CDR versus sampling clock rms jitter for different phase steps and zero preamble bits.

given signal-to-noise ratio (SNR), the same cannot be implied about the PLR performance, which is dependent on the delimiter being correctly identified. Consequently, the BER may not be a true reflection of the system performance, but that of the properly received bursts only, as many other bursts may be lost without being included in the BER measurement.

The PLR performance can be improved by increasing the error resistance of the pattern correlator with a more sophisticated design of the pattern correlator. Thus, the complexity of the pattern correlator depends on an acceptable error resistance of the delimiter. Consider Fig. 13(a), where we plot (39), i.e., the PLR performance P_{l_z} , as a function of the BER P_e for different error resistance values z of the delimiter. Even with a simple pattern correlator having no error resistance ($z = 0$ bits), we obtain error-free operation: $\text{PLR} < 10^{-9}$ at $\text{BER} = 10^{-10}$. Furthermore, by increasing the pattern correlator error resistance to $z = 1$ bit, we obtain an improvement in the PLR performance by eight orders of magnitude.

In Fig. 13(b), we plot the PLR performance of the BM-CDR as a function of the rms jitter on the sampling clock for the worst-case phase step and zero preamble bits. As expected, the PLR performance degrades with increasing rms jitter; however, by increasing the error resistance of the pattern correlator, there is considerable amount of improvement in the PLR performance at a given rms jitter, while the allowable rms jitter increases for a given PLR.

E. Effect of Frequency Offset

To study the effect of frequency deviation of the sampling clock (LO) from the desired data rate on the BER and PLR performance of the BM-CDR, consider the plot shown in Fig. 14(a) resulting from (36) and (38). We set the length of CIDs $m = 0$, and assume that the CDR is using both the rising and falling edges of the input data to adjust the clock phase, thus $k = 2$. We vary the frequency offset parameter Δf and determine its effect on the phase error between successive packets $\Delta\varphi_e$ and

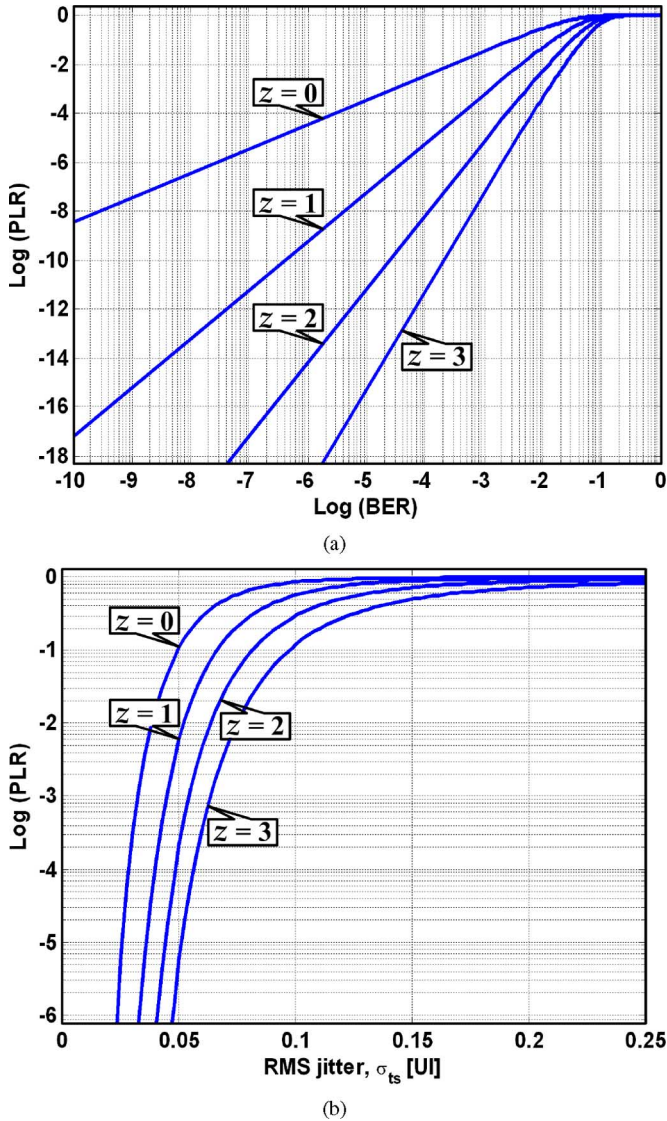


Fig. 13. Effect of pattern correlator error resistance on the PLR performance versus. (a) BER performance and (b) rms jitter on the sampling clock.

the sampling clock rms jitter σ_{t_s} . Plugging these parameters in (34) and (39), we can determine the BER and PLR performance of the BM-CDR, respectively. It can be seen that the BM-CDR achieves error-free operation for a frequency lock range of 590 MHz, i.e., from -295 to $+295$ MHz. This is obviously an optimistic result as the model does not account for the jitter generated by the circuit that would deteriorate the result appreciably. This will be further elaborated upon when presenting the experimental results in Section VIII-D. After this lock range, any further increase in the frequency offset will degrade the performance.

Next, we determine the maximum length of CIDs m_{\max} that can be tolerated by the CDR and the BM-CDR in the presence of a frequency offset. In Fig. 14(b), we plot (37). As can be expected in general, the tolerance to CIDs decreases with increasing frequency deviation

$$\lim_{|\Delta f| \rightarrow \infty} m_{\max} = 1. \quad (42)$$

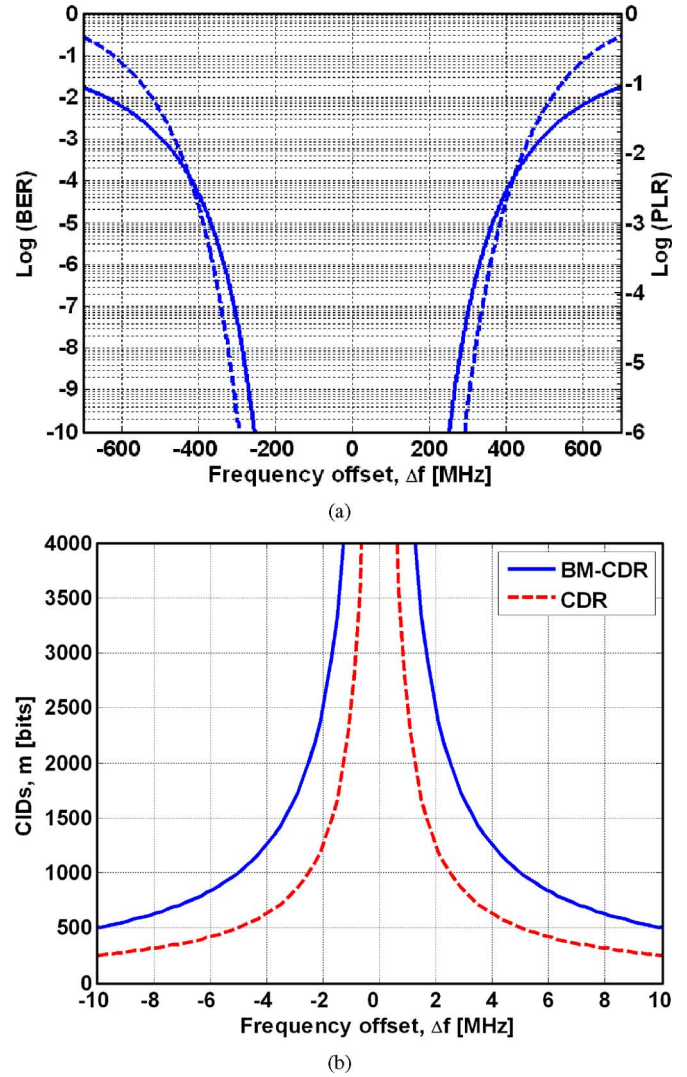


Fig. 14. (a) BER and PLR performance of BM-CDR versus frequency offset (solid lines for BER curves; dashed lines for PLR curves). (b) Maximum length of CIDs tolerated by the CDR and the BM-CDR versus frequency offset.

However, it can be inferred from Fig. 14(b) that the BM-CDR is able to tolerate significantly more CIDs than the CDR at lower frequency deviations.

VI. BM-CDR DESIGN AND IMPLEMENTATION

In this section, we present the design of the BM-CDR proposed in Section III and its detailed hardware implementation.

A. Overall Design

1) *Building Blocks*: The main building blocks of the BM-CDR we designed are illustrated in Fig. 15. The BM-CDR is essentially composed of a multirate CDR and a CPA module implemented on a Virtex IV field-programmable gate array (FPGA) from Xilinx. The multirate CDR comprises a clock recovery unit (CRU) from Centellax (Part #TR1C1-A) and a data sampler from Inphi (Part #13701DF), both rated at 13 Gb/s. The multirate CDR recovers the clock and data from the incoming signal. The CDR supports the following frequencies

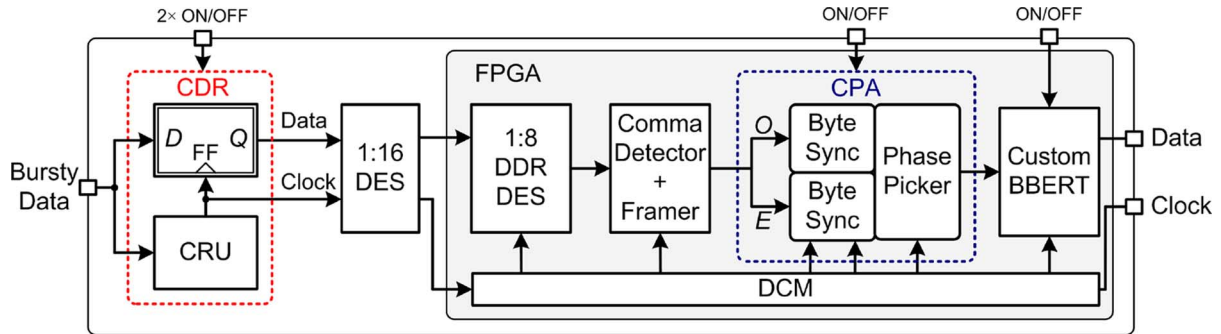


Fig. 15. Block diagram of the BM-CDR (BBERT: burst bit error rate tester; CDR: clock and data recovery; CPA: clock phase aligner; CRU: clock recovery unit; DCM: digital clock manager; DES: deserializer; FF: flip-flop; FPGA: field-programmable gate array; and Sync: synchronizer).

of interest: 1) 5 Gb/s for conventional mode and 2) 10 Gb/s for two-times oversampling and BM. The CDR is followed by a 1 : 16 deserializer (DES) from Maxim-IC (Part #MAX3950) rated at 10.3 Gb/s. The deserializer reduces the frequency of the recovered clock and data to a lower frequency that can be processed by the digital logic. The lower rate 16-bit parallel data and the divided clock are then brought onto the FPGA for further processing. The maximum data rate supported by the low-voltage differential signaling (LVDS) buffers of the FPGA is 840 Mb/s. Thereafter, a double-data rate (DDR) 1 : 8 DES, a framer, a comma detector, the CPA (including byte synchronizers and a phase picker), and a digital clock manager (DCM) are implemented on the FPGA alongside a custom burst BER tester (BBERT). A computer is used to communicate with the BBERT.

On the board, it is first necessary to further parallelize the data and clock to a lower frequency that will ensure proper synchronization and better stability of these signals before they can be sent to the CPA for automatic phase acquisition. Thus, an integrated DDR 1 : 8 DES is implemented on the FPGA, which will be elaborated upon in the next section. Automatic detection of the payload is implemented on the FPGA through a framer and a comma detector that are responsible for detecting the beginning (delimiter bits) and the end (comma bits) of the packets, respectively. As described in Section III-A, the CPA makes use of a phase-picking algorithm and a CDR operated in two-times oversampling mode. The CPA is turned ON for BER and PLR measurements with phase acquisition for BM reception ($\Delta\varphi \neq 0$ rad); otherwise, it can be bypassed for continuous-mode reception ($\Delta\varphi = 0$ rad). The realigned data are then sent to the custom BBERT, which will be detailed in Section VI-C.

2) *Implementation Details:* A photograph of the current implementation of the BM-CDR is shown in Fig. 16. The 1 : 16 DES evaluation board uses a SubMiniature version B (SMB) connector rated at 4 GHz, whereas the FPGA evaluation board uses a high-speed micro Q-strip interface socket (QSE) connector. The QSE connector is from Samtec (Part #QSE-040-01-L-D-A), rated at 8 GHz (differential signaling). Since the outputs of the DES and the inputs of the FPGA both use LVDS logic, no conversion other than a connector conversion is needed at the interface between the two. Note the custom SMB-to-QSE interface printed circuit board (PCB) that sits between the deserializer and the FPGA in Fig. 16. We used 34 6-in SMB

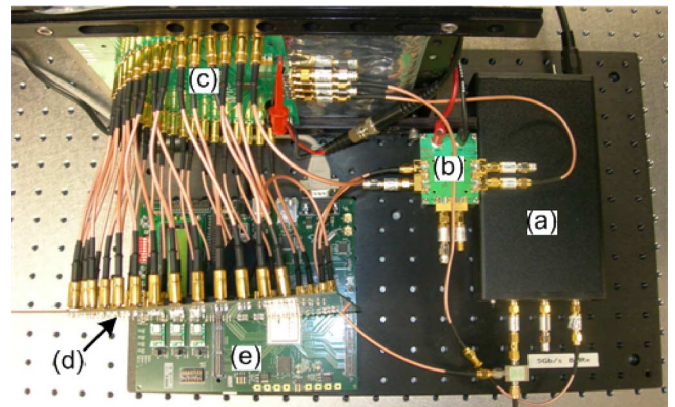


Fig. 16. Photograph of the current implementation of the BM-CDR. (a) CRU, (b) data sampler, (c) 1 : 16 DES, (d) Custom SMB-to-QSE interface PCB, and (e) FPGA.

cables (16-bit differential data + 1 differential clock) to connect the DES outputs to the SMB-to-QSE interface PCB, and a high-speed parallel mating cable from Samtec (Part #EQCD-040-06.00-TTR-TBL-1) rated at 1.74 GHz to complete the connections to the FPGA. Note that the SMB-to-QSE interface PCB would not be part of a commercial product and would not be needed if the main blocks were integrated on a single PCB or a single application-specific IC (ASIC).

B. Data Deserialization

The main challenge in designing gigabit-capable receivers based on FPGAs is the limited processing speed of digital logic on commercially available FPGAs. For example, the DCM module on the FPGA, in essence of a digital PLL, is limited to an operating range of 24–500 MHz. The latter frequency is 20 times slower than the targeted 10 Gb/s (two-times oversampling of the 5-Gb/s data). Thus, two stages of deserialization are employed. Note that the DCM, an intellectual property (IP) block from Xilinx, is a key design component that provides multiple phases of a source clock and a zero propagation delay with low clock skew between the output clock signals distributed throughout the board.

The first deserialization stage is performed by the offboard 1 : 16 deserializer. The oversampled 10-Gb/s data and clock are deserialized to 34 parallel signals (16 differential data signals +

1 differential clock signal), each at 625 Mb/s each. These signals are then brought on to the FPGA board through LVDS logic. The maximum data rate supported by the LVDS buffers of the FPGA is 840 Mb/s, well above (by 215 Mb/s) the deserialized signal data rate. However, the 625-MHz clock signal is $1.25\times$ faster than the maximum operating frequency of the DCM, which is 500 MHz. Thus, a clock divider is used to reduce the frequency of the received clock to 312.5 MHz. This clock signal is then fed to the DCM block for further clock distribution throughout the system.

The second deserialization stage is based on the DDR signaling, and it is accomplished by a 1 : 8 deserializer designed and implemented on the FPGA. It uses the 312.5-MHz DCM output clock signal to sample the 625 Mb/s incoming data at both the rising and the falling clock edges—DDR signaling. In this way, each data signal is separated into two data lines by a half-rate clock signal. The same clock is then used to demultiplex these two lines of data into an 8-bit data path. In summary, the 16 input data signals are deserialized to 128 data lines at ~ 78 Mb/s, which is eight times lower than 625 Mb/s. The advantage of this method is that the clock signal is well within the 24–500 MHz operating range of the DCM, guaranteeing system synchronization while keeping the same harmonic content of the clock and data lines.

C. Burst BER Tester

The FPGA-based BBERT designed is implemented to selectively perform BER and PLR measurements on the payload of the packets only. The BERT compares the incoming data, a pseudorandom binary sequence (PRBS), with an internally generated PRBS. Note that, while a conventional BERT can be used to make the BER measurements, PLR measurements on discontinuous, bursty data are not supported. This is because conventional BERTs require a continuous alignment between the incoming pattern and the reference pattern, and milliseconds to acquire synchronization. The phase step response of the BM-CDR can make conventional BERTs lose pattern synchronization at the beginning of every packet while the sampling clock is being recovered by the CDR. The custom BERT does not require fixed synchronization between the incoming pattern and the reference pattern of the error detector. Synchronization happens instantaneously at the beginning of every packet, thus enabling PLR measurements on discontinuous, bursty data.

There are a total of 19 counters on the FPGA to keep track of the PLR and the BER. A total of 16 counters are used to count the number of errors in the deserialized data. The three remaining counters keep track of the number of packets received, the number of bits received, and the number of packets lost, respectively. We used MATLAB to compute and display the PLR and the BER in real time, and we used HyperTerminal to control and monitor the state of the BM-CPA. Both communicate with the FPGA core through the RS-232 protocol. In order to selectively perform BER measurements on the payload of the packets, we used the delimiter and the comma as gating signals for the 16 error counters. The 16-bit parallel data are compared with the PRBS loaded into a memory block of the FPGA. The

memory address is incremented each time a new 16-bit vector is clocked in. It is reset to zero when the comma is detected in order to arm the BBERT for the next packet. The packet and packet lost counters are always enabled. Since the comma is far away from the beginning of the packet, it is always detected. Moreover, we used a long comma (48 bits) in order to reduce the probability of getting a false positive. The packet counter is incremented every time a comma is detected. The packet lost counter is incremented when a comma does not pair up with a previously received delimiter. This situation arises when the CDR was not given a preamble long enough to recover the phase before the arrival of the delimiter. When a packet is lost, it does not contribute to the BER. Hence, a zero BER does not mean that there are no errors. Both the PLR and the BER must be monitored while measuring the phase acquisition time.

VII. EXPERIMENTAL SETUP

This section describes the BM experimental setup, test signal specification, and measurement methodology used to test and characterize the BM-CDR in a 20-km PON uplink.

A. BM Test Setup—PON Test Bed

The BM experimental test setup (BM-TS) illustrated in Fig. 17 is used to test the BM-CDR in a 20-km PON uplink. Bursty upstream PON traffic is generated by adjusting the phases φ_1 and φ_2 between alternating packets from two programmable ports of an Anritsu MP1800A pattern generator, which are then used to drive their respective polarization-dependent Mach-Zehnder modulators (MZMs). The amplitude of the packets A_1 and A_2 is adjusted by employing variable optical attenuators (VOAs) at the output of each 1310-nm Fabry-Perot (FP) lasers. The launch power is set to 0.5 dBm with an extinction ratio of 10 dB as per the GPON standard [7]. These packets are formed from guard bits, preamble bits, delimiter bits, $2^{15} - 1$ PRBS payload bits, and comma bits. As per (3), a silence period T_s consisting of a phase step $|\Delta\varphi| = |\varphi_1 - \varphi_2| \leq 2\pi$ rad and an all-zero sequence of m CIDs can be inserted between the packets. Note that the phase steps between the consecutive packets can be set anywhere between ± 250 ps with a 1-ps resolution corresponding to a ± 1.25 UI at 5 Gb/s. The packets from the two ONUs are then coupled and sent over a 20-km single-mode fiber (SMF-28) uplink. A VOA serves to control the received power level. At the OLT, the optical-to-electrical conversion is performed by a p-i-n photodiode from New Focus (Model #1434). The bursty signal is then low-pass filtered before being sent to the BM-CDR. The LPF is a fourth-order Bessel-Thomson filter from Picosecond to remove out-of-band high-frequency electrical noise whose -3 -dB cutoff frequency is $0.75 \times$ bit rate or 3.75 GHz. Such a filter has an optimum bandwidth to filter out noise while keeping ISI to a minimum [32]. Eye diagrams of the bursty traffic at the input to the BM-CDR are shown in Fig. 17.

B. Test Signal Specification

The IEEE 10G-EPON task force is currently engaged in detailed discussions aimed at standardizing the physical

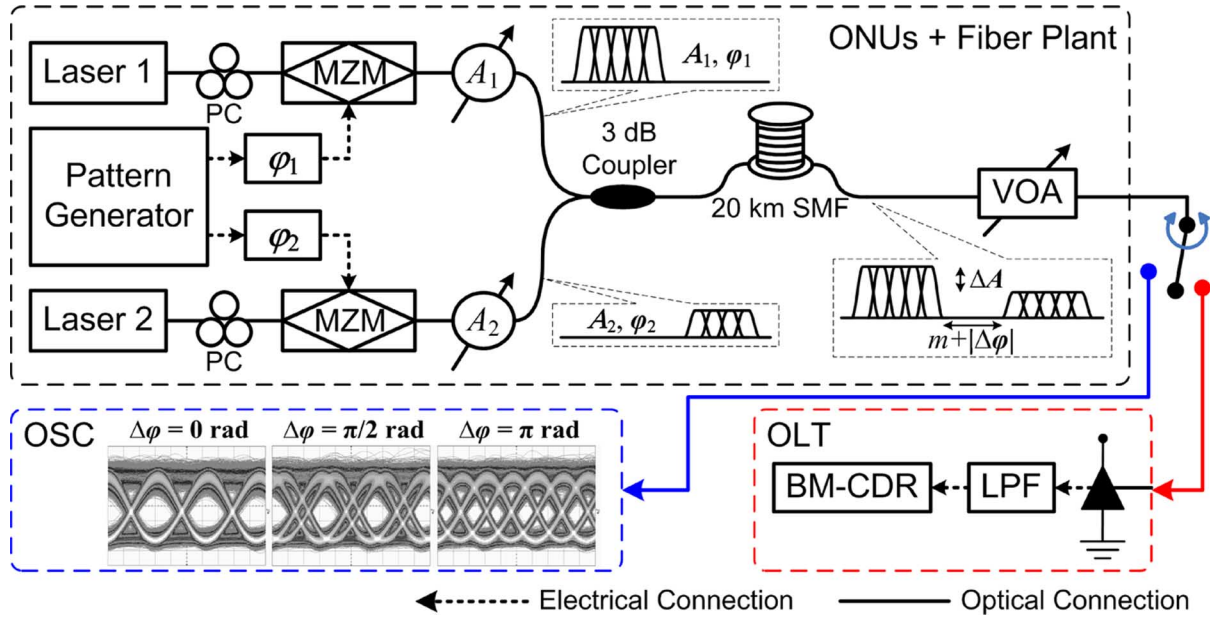


Fig. 17. BM experimental setup to test and characterize the BM-CDR in a 20-km PON uplink. Details of the test signal and BM-CDR are depicted in Figs. 15 and 18, respectively (BM-CDR: burst-mode clock and data recovery; LPF: low-pass filter; MZM: Mach–Zehnder modulator; OLT: optical line terminal; ONUs: optical network units; OSC: oscilloscope; PC: polarizer controller; SMF: single-mode fiber; VOA: variable optical attenuator).

TABLE II
UPSTREAM BM OVERHEAD PON PARAMETERS

	Data Rate [Mb/s]	Guard Time [bits]	Preamble [bits]	Delimiter [bits]
GPON	1244.16	32	44	20
	2488.32	64	108	20
GEPON	1250	1280	1040	32

specifications to attain a total bandwidth of 10 Gb/s [33]. Since the 10 G-EPON is backward compatible with GEPON [6], the timing parameters are assumed to be closely related. Table II compares the upstream BM overhead parameters for GEPON and GPON [7]. While our BM-CDR is compatible with both standards, we have nonetheless decided to test the BM-CDR under the stringent timing requirements imposed by the latter. A typical bursty signal that complies with the GPON standard is used as a test signal in our experiments and is depicted in Fig. 18. Packet k , with amplitude A_k , and phase φ_k , consists of 64 guard bits, 0–108 (l) preamble bits, 20 delimiter bits, $2^{15} - 1$ payload bits, and 48 comma bits. The guard, preamble, and delimiter bits correspond to the physical-layer upstream BM overhead of 24 bytes. The guard bits provide distance between two consecutive packets to avoid collisions. The preamble is split into two fields, a threshold determination field (TDF) for amplitude recovery and a CPA field for clock-phase recovery. The delimiter is a unique pattern indicating the start of the packet to perform byte synchronization. Likewise, the comma is a unique pattern to indicate the end of the payload. The payload is simply an NRZ $2^{15} - 1$ PRBS with a zero appended at the end. The PLR and the BER are measured on the payload bits only.

C. Measurement Methodology

In our BM-TS, we can set the amplitude and relative phase of the packets, the preamble length, the length of CIDs, and control the received signal power. This consequently makes it possible to fully and correctly characterize CDRs and BM-CDRs—the device under test (DUT). In this context, we outline the following measurement methodologies.

1) *Phase Acquisition Time*: To measure the phase acquisition time accurately, packet 1 is made to serve as a dummy packet to force the DUT to lock to a certain phase φ_1 before the arrival of packet 2 with phase φ_2 . The CID length is set to zero for this measurement. The BER and PLR measurements are made on packet 2 only. For a given phase step $|\Delta\varphi| \leq 2\pi$ rad, we measure the lock acquisition time of the DUT by increasing the length of the preamble l , until we obtain error-free operation, which we define as a BER $< 10^{-10}$ and a PLR of zero for over 3 min at 5 Gb/s ($> 30^6$ packets received). As already explained in Section V-B, this method of measuring the phase acquisition time is more accurate than the qualitative method of monitoring the CDR's VCO control voltage [34]. In the latter case, the phase acquisition time is determined by measuring the settling time of the VCO control voltage envelope to within a certain percentage (usually 2%–5%) of the steady-state value. The drawback of this method is that it overestimates the lock acquisition time as it is not necessary for the clock to be perfectly aligned with the data before the payload becomes valid.

2) *CID Immunity*: We measure the CID immunity of the DUT by inserting m 0's between the consecutive packets until error-free operation can no longer be maintained. The preamble length is set to zero for this measurement. The phase step can be varied to observe the effects on the CID immunity. In this case,

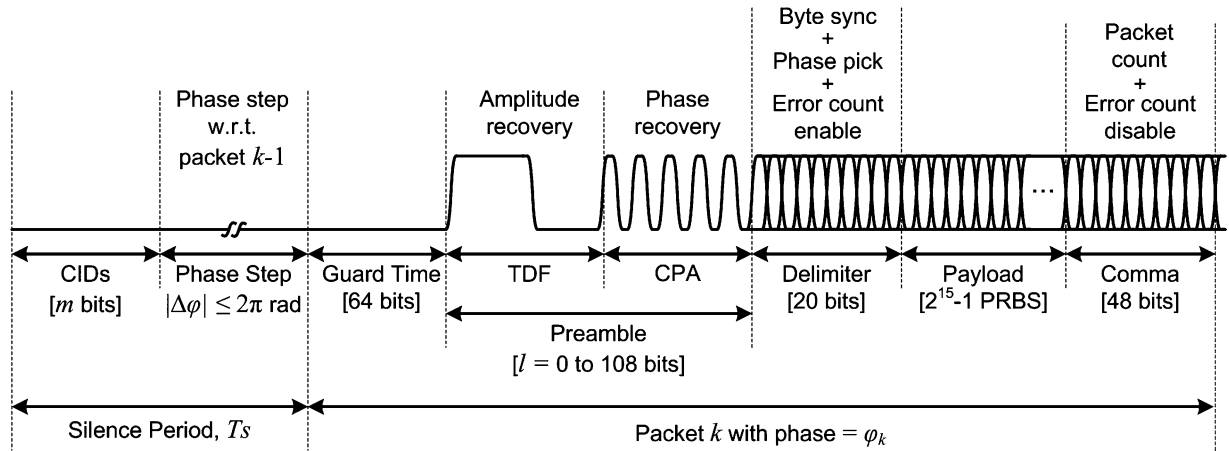


Fig. 18. Typical BM uplink test signal and specification at 5 Gb/s (CIDs: consecutive identical digits; CPA: clock phase alignment; PRBS: pseudorandom binary sequence; TDF: threshold determination field).

packet 1 is made to serve as a dummy packet, while BER and PLR measurements are made on packet 2 only.

3) *Frequency Acquisition Range*: The frequency lock range of the DUT is measured by tuning the frequency of the VCO away from the desired bit rate until error-free operation can no longer be maintained. The effect of phase steps can also be examined; however, the preamble length and CID length are both set to zero for this measurement.

4) *Sensitivity Measurements*: Sensitivity measurements of the DUT are made possible by adjusting the power level of the received packets until error-free operation can no longer be maintained. The CID length is set to zero for this measurement; however, the preamble length and phase step can both be varied to measure the BM sensitivity penalty.

5) *Dynamic Range*: Finally, to measure the dynamic range of the DUT, we fix the amplitude A_1 of packet 1, and increase or decrease the amplitude A_2 of packet 2, until the DUT can no longer maintain error-free operation on packet 2. The phase step, preamble length, and CID length are all set to zero for this measurement.

VIII. EXPERIMENTAL RESULTS AND DISCUSSION

This section is devoted to the presentation and analysis of the experimental results obtained by testing our BM-CDR in the 20-km PON uplink test bed. We investigate the effect of phase step between consecutive packets, received signal power, frequency offset between the sampling clock and the desired bit rate, and length of CIDs, on the BER and PLR performance of the BM-CDR. We characterize the BM-CDR in terms of the phase acquisition time, burst-mode sensitivity penalty, frequency lock range, CID immunity, and dynamic range. Where appropriate, comparisons have been made with the predictions from the theoretical analysis in Section V, thereby validating the probabilistic theoretical model in Section IV.

A. Phase Acquisition Time

Here, we study the PLR performance of the CDR and the BM-CDR as a function of the phase step $|\Delta\varphi| \leq 2\pi$ rad with

no preamble bits. Note that 1 UI or 2π rad corresponds to 200 ps at 5 Gb/s. The methodology for measuring the phase acquisition time is delineated in Section VII-C. As shown in Fig. 19(a), with only the CDR (CPA turned OFF) we observe, as expected, two bell-shaped curves centered at approximately ± 100 ps because these represent the half-bit periods corresponding to the worst-case phase steps at $\Delta\varphi = \pm\pi$ rad, respectively. It follows that the CDR is sampling at the edge of the data eye, resulting in a PLR ~ 1 . We note that the slight shift of 4-ps from ± 100 ps is attributed to the sampling point of the recovered clock not being exactly at the center of the data eye. This may be as a result of: 1) VCO phase noise due to jitter generation by the CDR circuit and 2) data bits being neither symmetric nor having the same slope for the rise and fall times leading to different distribution of jitter on the edges of the data bits. At relatively small phase steps (near 0 or $\pm 2\pi$ rad), we can easily achieve zero PLR because the CDR is sampling near the middle of each bit. Preamble bits (“1010...” pattern) can be inserted at the beginning of the packets to help the feedback loop of the CDR settle down and acquire lock. As the preamble length is increased, there is an improvement in the PLR. After 50 preamble bits, as also explained in Section V, we perceive error-free operation for any phase step. However, the use of the preamble reduces the effective throughput and increases delay. On the other hand, by switching ON the BM functionality of the receiver with the CPA, as illustrated in Fig. 19(b), we observe error-free operation for any phase step with zero preamble bits, allowing for instantaneous phase acquisition. This is as predicted by the theoretical model.

It should be noted that although $|\Delta\varphi| = \pi$ rad represents the worst-case phase steps for the CDR sampling at the bit rate, $|\Delta\varphi| \in \{\pi/2 \text{ rad}, 3\pi/2 \text{ rad}\}$ phase steps are the worst-case scenarios for the BM-CDR as it is based on an oversampling CDR at twice the bit rate. We note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [10], [13]. However, by reducing the phase acquisition time as demonstrated in this paper—and therefore, the length of the CPA field—more bits are left for amplitude recovery, thus reducing the BM

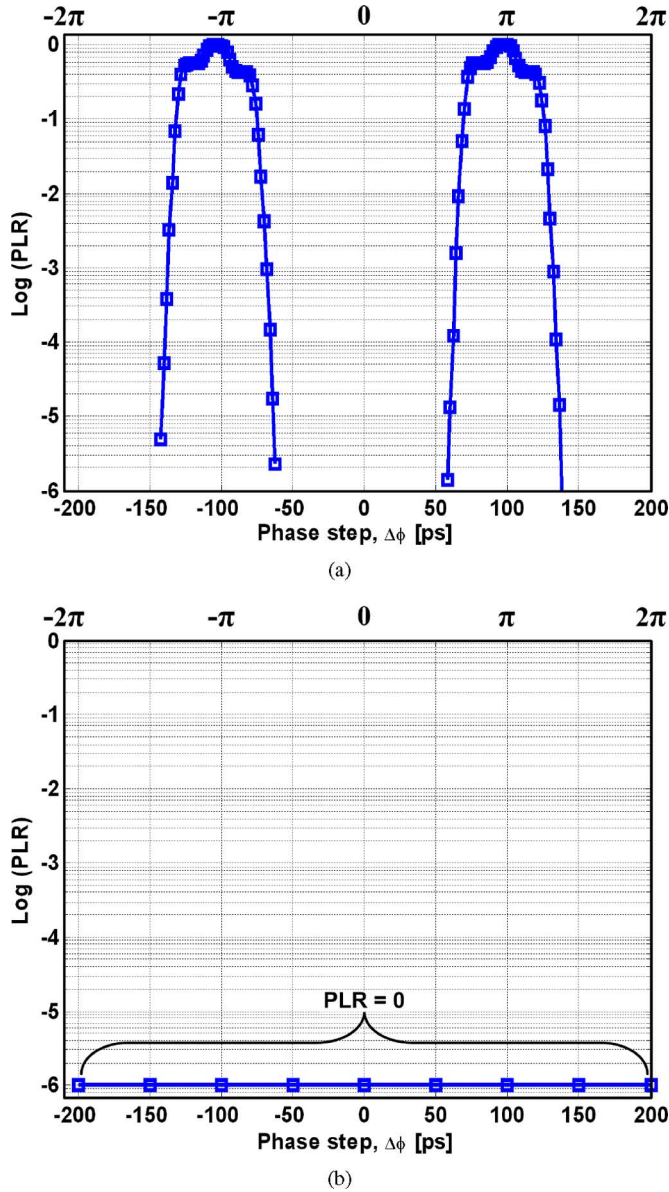


Fig. 19. PLR performance versus phase step for a zero preamble length. (a) Conventional CDR. (b) BM-CDR.

sensitivity penalty. Alternatively, with the reduced number of preamble bits, more bits can be left for the payload, thereby increasing the information rate. Instantaneous phase acquisition also has a significant improvement impact in the physical efficiency of the upstream PON traffic. This is further discussed in Section VIII-C.

In Fig. 20, we compare the experimental and theoretical PLR performances of the CDR with no preamble bits. We have restricted the horizontal axis to values from $0 \leq \Delta\varphi \leq 2\pi$ rad (0 to 200 ps), as the results are symmetrical about 0 rad from $-2\pi \leq \Delta\varphi \leq 0$ rad. We first evaluate the PLR performance obtained in the PON architecture with the 20 km of fiber to the one in a back-to-back (B2B) configuration without the fiber. The “flatness” of the curve near the worst-case phase step $\Delta\varphi = \pi$ rad in the PON architecture is a manifestation of the

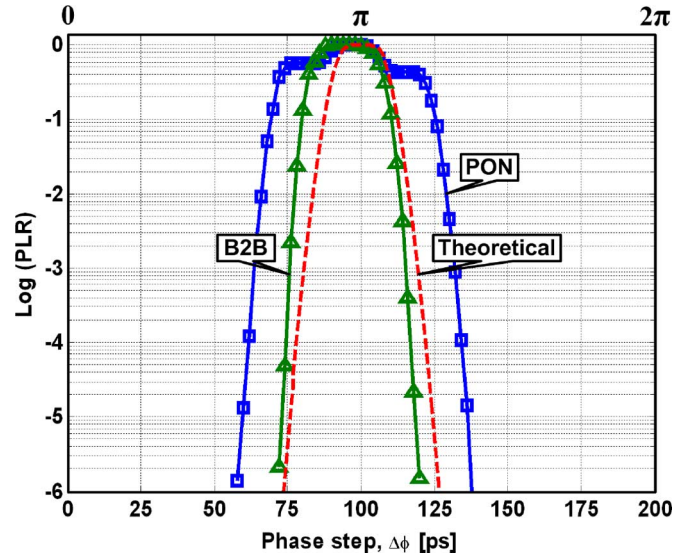


Fig. 20. PLR performance of the CDR versus phase step with no preamble bits in a B2B- and PON architecture, compared to the theoretical model.

presence of deterministic jitter as a result of channel impairments. This may include ISI, PWDJ, and DDJ. Next, we compare these results with the theoretical model by plotting (39) with the rms jitter on the sampling clock $\sigma_{t_s} = 0.025$ UI. It can be seen that the curve spread of PLR performance in the B2B architecture is $9.8 \sigma_{t_s}$ at $\text{PLR} = 10^{-6}$, whereas that obtained theoretically is $10.6 \sigma_{t_s}$. This signifies that the results are in close agreement, albeit for the 4 ps shift in the experimental plots due to the nonideal sampling point location determined by the CDR, which as mentioned is most likely due to the VCO phase noise.

B. BM Sensitivity Penalty

Consider the experimental results in Fig. 21, which shows the BER and PLR performance of the CDR and the BM-CDR as a function of the received signal power for different phase steps. Note that the abscissa is the useful power, i.e., the optical power contributed at the photodiode. To determine the BM penalty of the receiver, the performance of the CDR sampling continuous data ($\Delta\varphi \in \{0 \text{ rad}, \pm 2\pi \text{ rad}\}$) at the bit rate is compared to the performance of the BM-CDR sampling bursty data with a worst-case phase step ($|\Delta\varphi| \in \{\pi/2 \text{ rad}, 3\pi/2 \text{ rad}\}$). Both measurements are made with a 0-bit preamble. Due to the two-times oversampling (faster electronics) and the phase-picking algorithm, we observe a 0.8 -dB penalty in the BER performance, as shown in Fig. 21(a); however, in the case of the PLR performance, the penalty is negligible due to the CPA as depicted in Fig. 21(b). It can also be observed that the BM-CDR achieves BER and PLR sensitivities of -24.2 and -25.4 dBm, respectively, for the worst-case phase steps in the link. On the other hand, the CDR will not be able to recover any packets if there exists a worst-case phase step, regardless of the received signal power, thus resulting in a $\text{PLR} \sim 1$. However, by increasing the length of the preamble, the PLR performance of the CDR will tend to be comparable to that obtained with zero

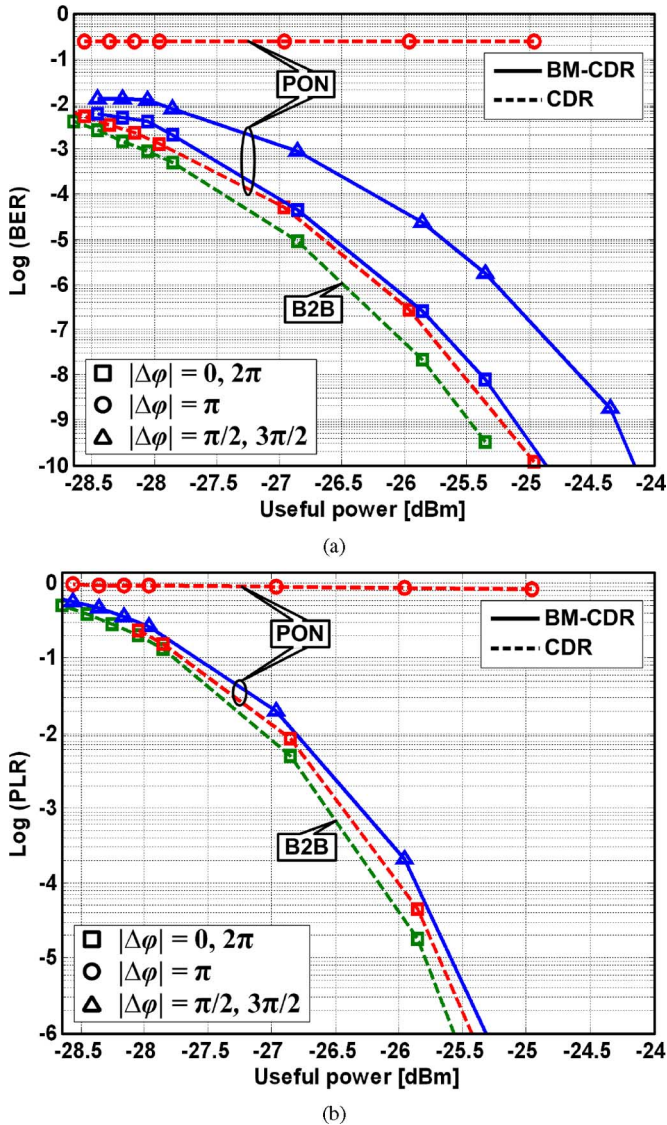


Fig. 21. BER and PLR performance of the CDR and the BM-CDR versus useful power in a B2B and PON architecture for different phase steps with no preamble bits.

preamble bits and no phase steps. Hence, for the worst-case phase steps in the uplink, there is a tradeoff between the sensitivity penalty obtained by employing the BM-CDR over the CDR and the number of preamble bits required without the BM-CDR. Since random silence periods in the PON uplink are inevitable, the power penalty may be a small price to achieve error-free operation.

It should also be noted that the sensitivity penalty, 0.4 dB and 0.14 dB in the BER and PLR performance, respectively, between the B2B and the PON architecture is minimal. This implies that the uplink does not need to be compensated by introducing dispersion compensation fiber (DCF), semiconductor optical amplifiers (SOA), or erbium-doped fiber amplifiers (EDFAs), as is generally necessary in a wavelength-division multiplexing (WDM) PON or optical code-division multiple access (OCDMA) PON [35].

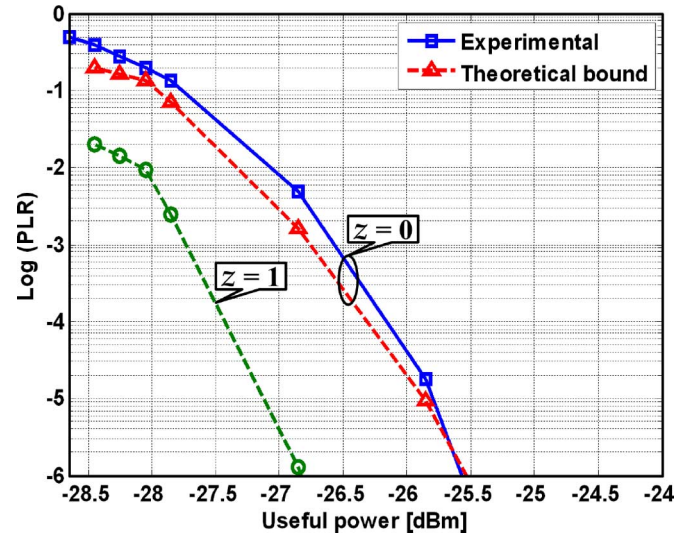


Fig. 22. Comparison of the theoretical and experimental PLR performances of the BM-CDR versus useful power.

We theoretically predict the PLR performance of the BM-CDR in the PON architecture as a function of the received signal power, with a pattern correlator having an error resistance of $z = 0$ bit, and compare it to the experimental result shown in Fig. 22. The theoretical and experimental results are in close agreement. By increasing the pattern correlator error resistance to $z = 1$ bit, an improvement of ~ 1.5 dB in the sensitivity can be expected.

C. PON Efficiency

Dynamic bandwidth allocation (DBA) is generally employed in high-speed communication services, such as a PON system, to effectively assign the shared resource on demand to each ONU according to their respective requests [36]. Several DBA algorithms for PONs have been proposed in the literature [37], [38], in which the upstream traffic is allocated according to the ONUs' request in every time cycle. In a PON link, the physical efficiency of the upstream traffic E_{us} is defined as [39]

$$E_{us} = 1 - \frac{n_{ONU} t_{oh}}{T_{DBA}} \quad (43)$$

where n_{ONU} is the number of ONUs in the PON, t_{oh} is the physical overhead time, and T_{DBA} is the cycle for bandwidth allocation. T_{DBA} can be expressed as

$$T_{DBA} = RTT + t_{delay} \quad (44)$$

where RTT is the round-trip time between the OLT and the ONU, and t_{delay} is the time required for bandwidth allocations other than the RTT . In a 20-km link, the round-trip time $RTT \sim 200 \mu s$ with light propagating at $\sim 5 \mu s/km$ in an SMF. Thus, the cycle for bandwidth allocation $T_{DBA} \geq 200 \mu s$. The overhead time t_{oh} is represented as

$$t_{oh} = t_{gt} + t_{pre} \quad (45)$$

where t_{gt} is the guard time between B2B upstream bursts from different ONUs and mostly dependent on the laser ON and OFF

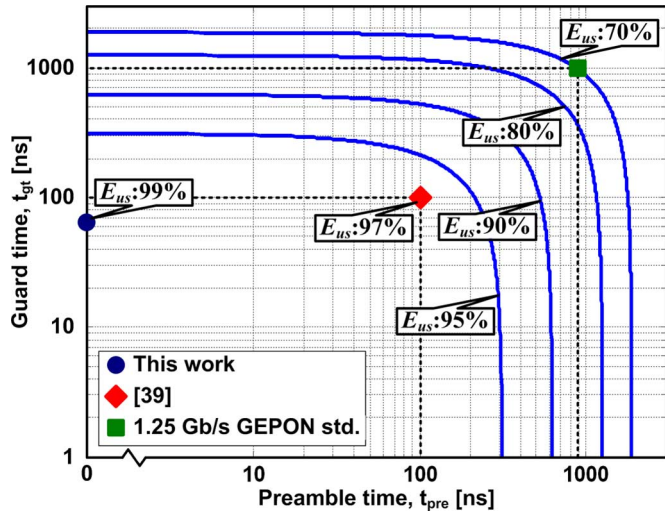


Fig. 23. Physical efficiency of the upstream PON traffic as a function of the preamble time and guard time.

times, and t_{pre} is the preamble time required for the BMRx to settle down and completely synchronize for each burst input in terms of the amplitude and the phase. In the GEAPON standard [6], the overhead time $t_{oh} = 1856$ ns, the guard time $t_{gt} = 1024$ ns, when the overlap between the laser ON and OFF times is not considered, and the preamble time $t_{pre} = 832$ ns, of which 400 ns is for the amplitude recovery and 432 ns is for the phase acquisition. Hence, assuming 32 ONUs, an upstream efficiency $E_{us} \sim 70\%$ is obtained for the GEAPON standard with a bandwidth allocation cycle $T_{DBA} = 200 \mu s$.

In Fig. 23, we plot contours of the PON upstream efficiency that result as a function of the required preamble time and guard time. Since our BM-CDR provides instantaneous (0 preamble bit) phase acquisition, a high upstream efficiency $E_{us} \sim 99\%$ is expected for 32 ONUs and $200\text{-}\mu s$ T_{DBA} . Compared to the GEAPON standard, this is a 24% improvement even though the bit rate is four times higher. The BM amplitude recovery circuit presented in [39] achieves an efficiency of 97%. In this context, our studies can seamlessly integrate, albeit with a 2% tradeoff in the upstream efficiency. In addition, note that the guard time is limited by the laser ON and OFF times. A shorter guard time and thus a higher upstream efficiency can be obtained when transmitters with faster response times become available.

D. Frequency Acquisition Range

We measure the frequency acquisition range of the BM-CDR with the methodology outlined in Section VII-C with the received signal power kept at -24 dBm. Fig. 24 shows the PLR performance of the BM-CDR in the presence of frequency offset. The frequency lock range of the BM-CDR is measured to be 242 MHz. Based on the theoretical analysis in Section V-E, the lock range (maximum bound) is estimated to be 590 MHz. This discrepancy of ~ 350 MHz that can be expected as the finite frequency offset model is an optimistic estimation as it does not account for the jitter generated by the CDR circuitry. Jitter generation refers to the jitter produced by a circuit itself when

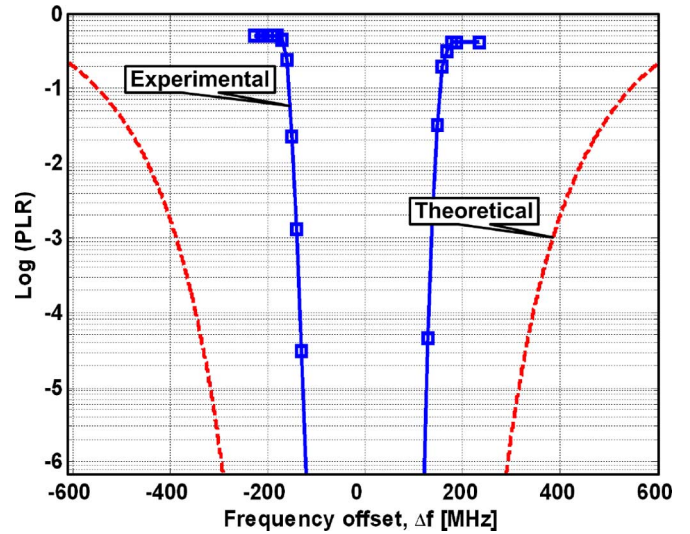


Fig. 24. Comparison of the theoretical and experimental PLR performances of the BM-CDR versus frequency offset.

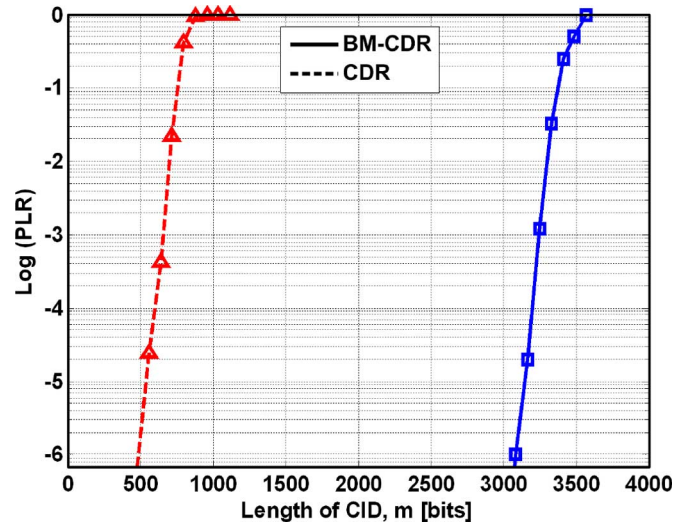


Fig. 25. PLR performance of the CDR and the BM-CDR versus length of CID.

the input random data contain no jitter. The sources of jitter are as follows [14]: 1) VCO phase noise due to electronic noise of its constituents devices; 2) ripple on the control voltage; 3) coupling of data transitions to the VCO through the phase detector and retiming circuits; and 4) supply and substrate noises. All these sources of jitter can considerably deteriorate the result.

E. CID Immunity

The PLR performance of the CDR and the BM-CDR as a function of the length of CIDs is depicted in Fig. 25. The CID immunity is measured with the methodology in Section VII-C. The received signal power is kept at -24 dBm. The CDR can only support 500 CIDs with error-free operation, whereas the BM-CDR can support approximately six times this value, i.e., 3100 CIDs. As the length of the CIDs is increased, the phase error between the two successive bursts can accumulate up to

TABLE III
SUMMARY OF BM-CDR PERFORMANCE COMPARED TO PREVIOUS WORK AND PON STANDARDS

	Previous Work						PON Standards		This Work
	[15]	[16]	[17]	[18]	[19]	[21]	GPON	GEAPON	
Data Rate	2.488 Gb/s	10.3 Gb/s	10.3 Gb/s	10 Gb/s	10 Gb/s	1.25 Gb/s	1.25 Gb/s	2.488 Gb/s	5 Gb/s
BER	N/A	$< 10^{-12}$	$< 10^{-12}$	N/A	$< 10^{-12}$	$< 10^{-12}$	$< 10^{-10}$	$< 10^{-10}$	$< 10^{-10}$
PLR	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	$< 10^{-6}$
Phase Acquisition Time	100 bits	N/A	1 bit	32 bits	5 bits	50 bits	540 bits	44 bits	0 bit
Frequency Lock Range	N/A	160 MHz	N/A	N/A	N/A	N/A	N/A	N/A	242 MHz
CID Tolerance	32 bits	N/A	160 bits	7 bits	31 bits	7 bits	5 bits	72 bits	3100 bits

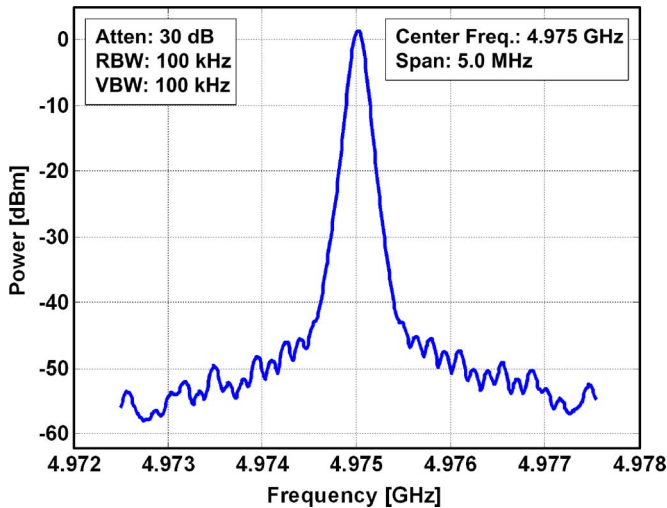


Fig. 26. Recovered clock spectrum (Atten: attenuation; Freq: frequency; RBW: resolution bandwidth; and VBW: video bandwidth).

$|\Delta\varphi_e| = \pi$ rad, resulting to a PLR ~ 1 . In the case of the CDR, this happens when the CID length is roughly a 1000 bits, while for the BM-CDR, it is 3500 bits. It can be inferred theoretically from Fig. 14(b) that a CID length of 3500 bits for the BM-CDR corresponds to a frequency offset of 1.73 MHz, implying a CID length of ~ 1600 bits for the CDR. While the experimental results and the theoretical results are within the same order of magnitude; there is, however, still a discrepancy. This is expected, as mentioned earlier, as the finite frequency offset model that does not account for the jitter generated by the circuit. It should be noted that in addition to the length of CIDs, when a worst-case phase step is introduced between consecutive packets, the CDR regardless of its CID immunity will result to a PLR ~ 1 . This is not the case with the BM-CDR, which, as demonstrated, is immune to any phase step between consecutive packets.

F. Dynamic Range

The methodology for measuring the dynamic range of a circuit is explained in Section VII-C. In a PON system, the BMRx front end at the OLT is responsible for amplitude recovery. Thus, the dynamic range of the BM-CDR does not carry much value. However, with the application of the BM-CDR to optical burst/packet-switched networks [40] that may require a cascade

of BM-CDR, the dynamic range of the BM-CDR may seem useful. In either case, the measurement of the dynamic range verifies the functionality of the BM-TS.

The worst-case scenario is when a low-amplitude packet follows a high-amplitude packet [41]. The dynamic range of the BM-CDR is measured to be 3 dB. This also relaxes the requirements of the output voltage swings/fluctuations from a preceding circuit at high data rates. The dynamic range can easily be increased to more than 15 dB by integrating a front end consisting of a BM amplitude recovery circuit [39].

G. Recovered Clock Spectrum

The output spectrum of the recovered clock is shown in Fig. 26. The phase noise at 100, 500, and 1000 kHz is approximately -40 , -77 , and -80 dBc/Hz, respectively. Note that the spectrum analyzer attenuates the input signal by 30 dB internally.

IX. SUMMARY AND CONCLUSION

We have proposed a 5-Gb/s BM-CDR circuit based on an oversampling CDR operated at twice the bit rate and a CPA that makes use of a simple, fast, and effective phase-picking algorithm for automatic clock phase acquisition. The BM-CDR inherits the low jitter transfer bandwidth and the low jitter peaking of the oversampling CDR. In addition, since the oversampling is achieved by employing a semiblind technique, a hybrid combination of phase tracking and blind oversampling, the jitter tolerance is the product of the individual jitter tolerances. Hence, the BM-CDR could also find applications in future high-speed optical burst/packet switched networks, which may require a cascade of BM-CDRs that each consumes some of the overall jitter budget of the system.

We developed a unified theoretical probabilistic model for the following: 1) conventional CDRs; 2) CDRs based on N times oversampling techniques in either time or space; and 3) BM-CDRs built from oversampling CDRs. This theory can quantitatively explain the performance of these circuits in terms of the BER and PLR. The model accounts for the following parameters: 1) silence period, including phase step and CIDs between successive upstream PON bursts from independent ONUs; 2) finite frequency offset between the sampling clock and data rate; 3) preamble length; 4) rms jitter on the sampling clock; and 5) pattern correlator error resistance. Based on this

theory, we also performed a comprehensive theoretical analysis to assess the tradeoffs between these parameters. Where appropriate, comparisons have been made with experimental results, thereby validating the theoretical model.

In summary, the jitter tolerance on the sampling clock of the CDR and the BM-CDR with no preamble bits at the worst-case phase step is predicted to be 0 and 0.02 UI, respectively. This implies that it is not feasible for the CDR to obtain instantaneous phase acquisition since a jitter-free sampling clock is practically impossible. By increasing the preamble length, the jitter tolerance for a given phase step increases. In the case of the CDR, at least 50 preamble bits are required to achieve error-free operation for any phase step; however, this comes at the cost of reduced effective throughput and increased delay. Due to the superior jitter tolerance of the BM-CDR, instantaneous phase acquisition for any phase step is possible. The PLR performance can be improved by increasing the error resistance of the pattern correlator with a more sophisticated design. With a simple pattern correlator having no error resistance, the model predicts a PLR $< 10^{-9}$ at BER = 10^{-10} . By increasing the error resistance to 1 bit, we observe an improvement of 1.5 dB at PLR = 10^{-6} and eight orders of magnitude at a given BER in the receiver sensitivity and PLR performance, respectively.

We experimentally investigated the effect of phase step, received signal power, frequency offset, and length of CIDs, on the BER and PLR performance of the BM-CDR in a 20-km PON uplink. Our BM test solution, aided by the new measurement methodology based on both BER and PLR, can measure the amplitude, frequency, and phase acquisition times of devices like SONET CDRs, BMRx amplitude recovery circuits, BM-CDRs, and frequency synthesizers. We characterized the BM-CDR in terms of the phase acquisition time, BM sensitivity penalty, frequency lock range, CID immunity, and dynamic range. Table III summarizes the performance of the BM-CDR, and compares it to other techniques reported in the literature and the PON standards. In a nutshell, the BM-CDR achieves a BER $< 10^{-10}$ and PLR $< 10^{-6}$ while featuring: 1) instantaneous (0 preamble bit) phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad; 2) BER and PLR sensitivities of -24.2 and -25.4 dBm, respectively; 3) negligible BM (phase acquisition) sensitivity penalty of 0.8 dB; 4) frequency acquisition range of 242 MHz; 5) CID immunity of 3100 bits; and 6) dynamic range of 3 dB. This analysis coupled with the experimental results will refine theoretical models of BMRx and PONs, and provide input for establishing realistic power budgets. Instantaneous phase acquisition can increase the effective throughput of the system by increasing the information rate, and also dramatically improve the physical efficiency of the upstream PON traffic to 99% for 32 ONUs. The price to pay to obtain instantaneous phase acquisition is faster electronics. On the other hand, our solution leverages the design of components for long-haul transport networks using low-complexity, commercial electronics, thus providing a cost-effective solution for PON BM-CDRs. These components are typically a generation ahead of the components for multiaccess networks. Thus, our solution will scale with the scaling for long-haul networks.

ACKNOWLEDGMENT

The authors would like to thank M. Zeng and N. Zicha for their technical assistance. The author (B. J. Shastri) is grateful to Dr. J. Faucher for helpful discussions. They would also like to thank the reviewers for their valuable comments.

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